STP3593 LF - ROX5242T1N Family

1.0 Description

Design is based on a Double-Oven OCXO construction.
It delivers an ultra-stable 10MHz sine wave frequency output over operating conditions.
It offers the capability to digitally control the frequency over the lifetime (when frequency accuracy is critical for the application).

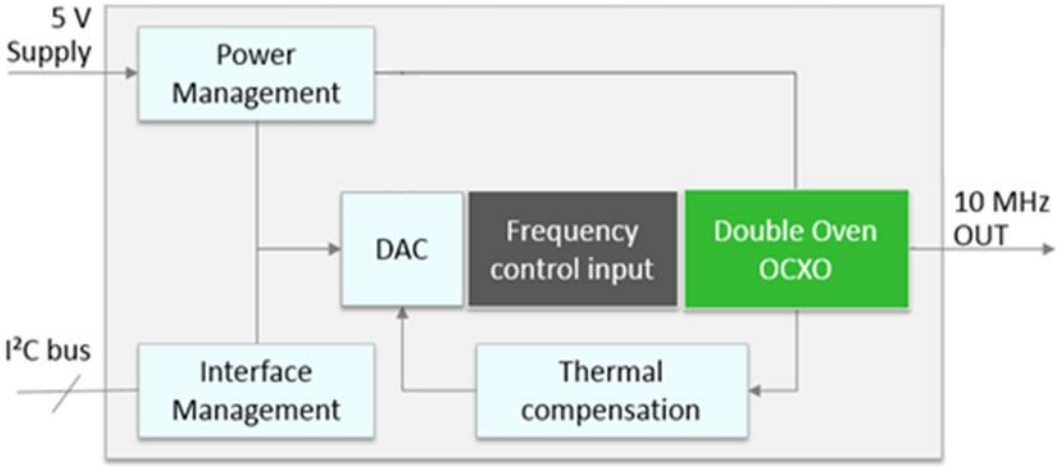
2.0 Application

- 5G Grand Master clock
- Stratum-2 clock replacement

3.0 Features

- Frequency Stability ≤ 50ppt peak to peak over operating range from -32°C to +70°C
- Package: 52 x 42 x 14 mm max
- 5V Single Power Supply
- 10 MHz sine wave output
- I²C bus data communication for Rakon settings & Digital Frequency Control (EFC) when frequency accuracy is needed.

Block Diagram



4.0 Absolute maximum ratings

Parameter	Min.	Max.	Unit
Storage temperature	-40	90	°C
Supply voltage (Vcc)	-0.3	6	V
Voltage at any Digital Interface Pin with Respect to GND	-0.3	Vcc +0.3	V
Load for sine wave RF output	45	55	Ω

5.0 Power Supply

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Supply voltage (Vcc)	4.75	5.0	5.25	V	
Current consumption (Warm up)			1500	mA	
Current consumption (Steady state)		600		mA	still air at 25°C
Power-on Recall Voltage	2.2			V	Minimum Vcc at which memory recall occurs
Vcc Ramp Rate	0.2			V/ms	

6.0 OCXO output

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Waveform	Sine wave				
Load	45	50	55	Ω	
Output Power	5	7	9	dBm	
Harmonics			-40	dBc	
Spurious			-80	dBc	
Start-up time			1	Second	

7.0 Temperature Range

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Operating temperature range	-32		+70	°C	Max airflow 2 m/s
Operable temperature range	-40		+85	°C	The oscillator will continue to provide an output signal, though not necessarily within the specified tolerances of frequency

8.0 OCXO Stabilization Steps

Warm-Up stage:

That stage corresponds to the initial operating mode of the device; it could occur after long powered-off period of time (storage, installation process, etc.).
Due to frequency recovery phenomenon, the device must be re-stabilized over continuous time of operation before reaching its overall intrinsic performances (up to 30 days maximum).

Stabilization steps & order of magnitude:

Start-up time within 1 second after powering-on the device; frequency signal output is delivered, within ppm of final frequency at that time.
Power consumption will stabilize within a couple of minutes after powering the device on at +25°C; that stabilization is dependent on ambient temperature at start (up to 5 minutes maximum at -40°C).

Temperature of the OCXO ovens will stabilize within less than 10 minutes after powering-on at -40°C.
Frequency stability versus time (ageing slope) will reach its final performance after recovery time (up to 30 days max. of continuous operation after powering-on).

9.0 Frequency Stability

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency		10.0		MHz	
Frequency calibration [1] @ +25°C ± 2°C	-50		+50	ppb	at time of shipment, with reference to nominal frequency
10 years life-time accuracy (overall)			± 350	ppb	After stabilization of the device (less than 30 days of continuous operation)
Frequency Stability Vs. Time (Aging)					After recovery time
Slope per day			± 0.2	ppb	Measured before shipment
per year			± 30	ppb	Cumulated (extrapolated)
for 10 years			± 300	ppb	Cumulated (extrapolated)
Frequency stability over temperature (-32°C to +70°C)		0.03	0.05	ppb	Reference to (F_{max} - F_{min})
Supply voltage stability	-0.01		+0.01	ppb	Nominal VCC ± 5% variation
Load sensitivity	-0.01		+0.01	ppb	50 Ω ± 10% variation
Acceleration sensitivity	-5	± 2.5	+5	ppb/g	Vs static orientation
Warm-up time @ 25°C			3	min	Within 10ppb in reference to final frequency after 1h of continuous operation
Warm-up time @ -40°C			5	min	Within 10ppb in reference to final frequency after 1h of continuous operation
Retrace Vs. operating temperature range		±1	±5	ppb	24h on, 24h off, 1h on
SSB Phase Noise with various offsets					dBc/Hz - Static conditions
1Hz		-100	- 95		
10Hz		-130	-125		
100Hz		-150	-145		
1kHz		-155	-150		
10kHz		-160	-155		
100kHz		-160	-158		
1MHz		-170	-165		
Short Term Stability (ADEV)					Static conditions
1s to 100s Tau		1.5	5	ppt	

10.0 Frequency Control

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
DAC value	0 Ox00000000	500 000 Ox0007A120	1 000 000 Ox000F4240	Dec value Hex value	
Frequency tuning	< -350	± 50	> +350	ppb	At shipment @ +25°C
Slope	0.7	0.8	0.9	ppt/step	
Linearity			± 10	%	

11.0 I²C Bus Interface

Signal Name	Type	Function	Notes	Logic Levels
I²C Data	Tristate Input / Output	Serial Data	Min 2kΩ external Pull-Up resistor to be connected to Vcc, conform to UM10204 NXP I²C-bus specification	While input to OCXO 3.8V < V_{IH} (High) < 5.3V V_{IL} (Low) < 0.4V While output to OCXO V_{OL} < 0.4V V_{OH} = OPEN
I²C Clock	Tristate Input	Serial Clock	Min 2kΩ external Pull-Up resistor to be connected to Vcc, conform to UM10204 NXP I²C-bus specification	3.8V < V_{IH} (High) < 5.3V V_{IL} (Low) < 0.4V
Frequency			400Hz max	

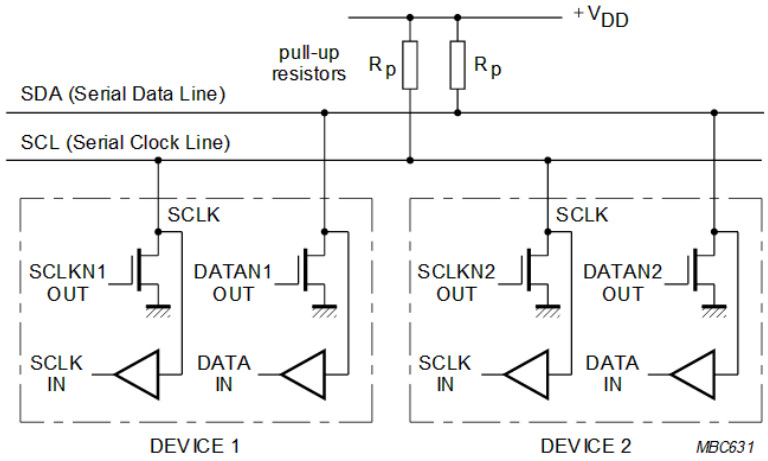
12.0 I²C Communication Conditions

I²C is not able to communicate in full-duplex mode, i.e. TX and RX are mutually exclusive. Rakon PPS Module acts as a slave in the communication setup, therefore they cannot initiate data transfers on their own. The host, which is always master, provides the data clock (SCL), and the clock frequency is therefore not configurable on the slave.

The I²C module is compliant with the Philips Semiconductors Inter-IC bus (I²C-bus) specification version 2.1. Fast mode up to 400 kbit/s. Fast-mode devices are downwards compatible i.e. they can be used in a 0 to 100 kbit/s Standard I²C-bus system.

Only two bus lines and a ground reference are required; a serial data line (SDA) and a serial clock line (SCL). The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400pF.

Master must handle clock stretching feature as stated in the Philips Semiconductors Inter-IC bus (I²C-bus) specification version 2.1 as I²C data might be delayed in case of critical timing sensitive computation.



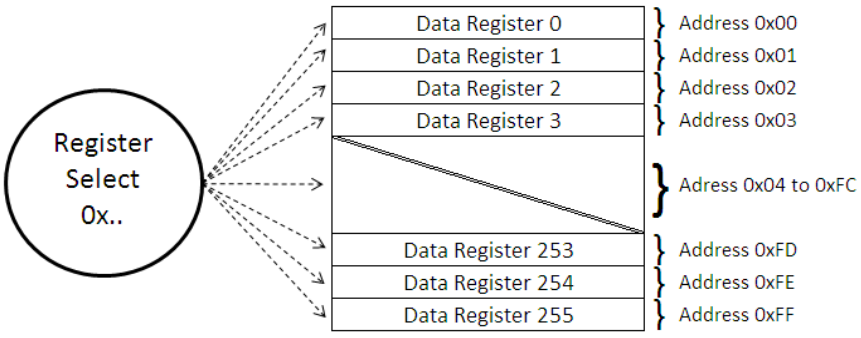
Connection of Standard- and Fast-mode devices to the I²C-bus.

It is generally known that the I²C bus can hang if an I²C master is removed from the bus in the middle of a data read. This can occur because the I2C protocol does not mandate a minimum clock rate. Therefore, if a master is reset in the middle of a read while a slave is driving the data line low, the slave will continue driving the data line low while it waits for the next clock edge. This prevents bus masters from initiating transfers. If this condition is detected, the following three steps will clear the bus hang condition:

1. An I²C master must generate up to 9 clock cycles.
2. After each clock cycle, the data pin must be observed to determine whether it has gone high while the clock is high.
3. As soon as the data pin is observed high, the master can initiate a start condition.

The receiver's I²C address is set to **0xE0** by default.

The I²C interface allows 256 slave registers to be addressed. As shown in Figure *I²C Register Layout* only a few of these are currently implemented. Others are reserved for future uses or internal computation and must not be addressed.



I2C Register Layout

Register detail

Next information will procure details regarding Rakon module register.
Slave Register: Refers to the address that has to be sent after the I²C slave address to select the desired register.
Description: Name and function of the register.
Firmware: Details on the firmware revision the register is supported on.
Comment: Additional information regarding the register or the data it represents.
Message Info: Number of bytes to be read and data type of the data register.

Slave Register	**0x3E**		
Description	Read Temperature Sensor		
Firmware	1.4+		
Comment	Represents an image of the external temperature seen by the NCO. The value can vary from Ox0000 to Ox0FFF, negative slope.		
Message Info	# bytes	Data-type	
	2	U-Short	

Slave Register	**0x41**		
Description	Read Frequency Control		
Firmware	1.4+		
Comment	Range can swing from Ox00000000 to Ox000F4240. 8E-13 typical frequency variation per step		
Message Info	# bytes	Data-type	
	4	U-Long	

Slave Register	**0x50**		
Description	Read Product Identification		
Firmware	1.4+		
Comment	Product traceability information ASCII format		
Message Info	# bytes	Data-type	
	64	Char	

Slave Register	**0x51**		
Description	Read firmware revision		
Firmware	1.4+		
Comment	Includes the name, version revision, release date and special parameters. ASCII format		
Message Info	# bytes	Data-type	
	64	Char	

Slave Register	**0xA0**		
Description	Write DAC 20 bits		
Firmware	1.4+		
Comment	Writing DAC value sweeping from 0 to 1 000 000. Hex value from Ox00000000 to Ox000F4240.		
Message Info	# bytes	Data-type	
	4	U-Long	

Slave Register	**0xC2**		
Description	Save frequency control value		
Firmware	1.4+		
Comment	Saves the value of the frequency control set with 0xA0 command. This value will be reloaded at start-up.		
Message Info	# bytes	Data-type	
	None	None	

13.0 Pin Connections

Parameter	Description
Pin 1	GND (mechanical and supply)
Pin 2	I²C Bus - SCL
Pin 3	I²C Bus - SDA
Pin 4	Supply Voltage (Vcc = +5.0V ± 5%)
Pin 5	RF Signal Output (10MHz Sine)

14.0 Marking

Parameter	Description
Type	Label marked
Barcode	Data matrix
Line 1	**RAKON**
Line 2	**STP3593 LF**
Line 3	10 MHz
Line 4	[SN: Lnnnnn] = Serial Number (1 * Letter + 5 * Numerals)
Line 5	[DC: YyWw] = date-code with 4 Digits for year / week

15.0 Manufacturing Information

Parameter	Description
Soldering	Hand or wave soldering
Assembly condition	Do not solder during upside down placement without mechanical fixation
Packaging description	All quantities will be provided in boxes
Moisture Sensitivity Level	MSL1 – Hermetically sealed package
Shelf life	No detrimental effect from a long shelf life (over 1 year). However, device requires up to 30 days max. of continuous operation prior to recovering its final stability versus time (ageing).

16.0 Environmental Specification[1]

Parameter	Description
RoHS	Parts are fully compliant with the European Union directives 2002/95/EC and 2011/65/EU on the restriction of the use of certain hazardous substances in electrical and equipment
Electro-Static Discharge	HBM (JESD22-A114 / 2kV) & CDM (JSESD22-C101 class C2 / 500V)
Latch-Up	Latch-up test (JESD78)
Mechanical Shocks	IEC 68-2-27 Test Ea. (50g, 11ms, ½ sine. 5 directions x 3 shocks)
Vibration	IEC 68-2-06 Test Fc. (10g, 10-500Hz 30 minutes/axis 1.5 hour total)
High Temperature Storage	HTSL @ +135°C / 1,000 hours (JESD22-A103)
Low Temperature Storage	LTSL @ -40°C 100 hours (JESD22-A119)
High Temperature Operating Life	HTOL @ +85°C 1,000 hours with Vcc=+5.25V (JESD22-A108)
Temperature Cycling Test	TCT : cycles from -40°C to +125°C (JESD22-A104): 500 cycles / 2 cycles per hour / 10 minutes soak time & transfer time less than 1 minute

[1] For qualification, not operational

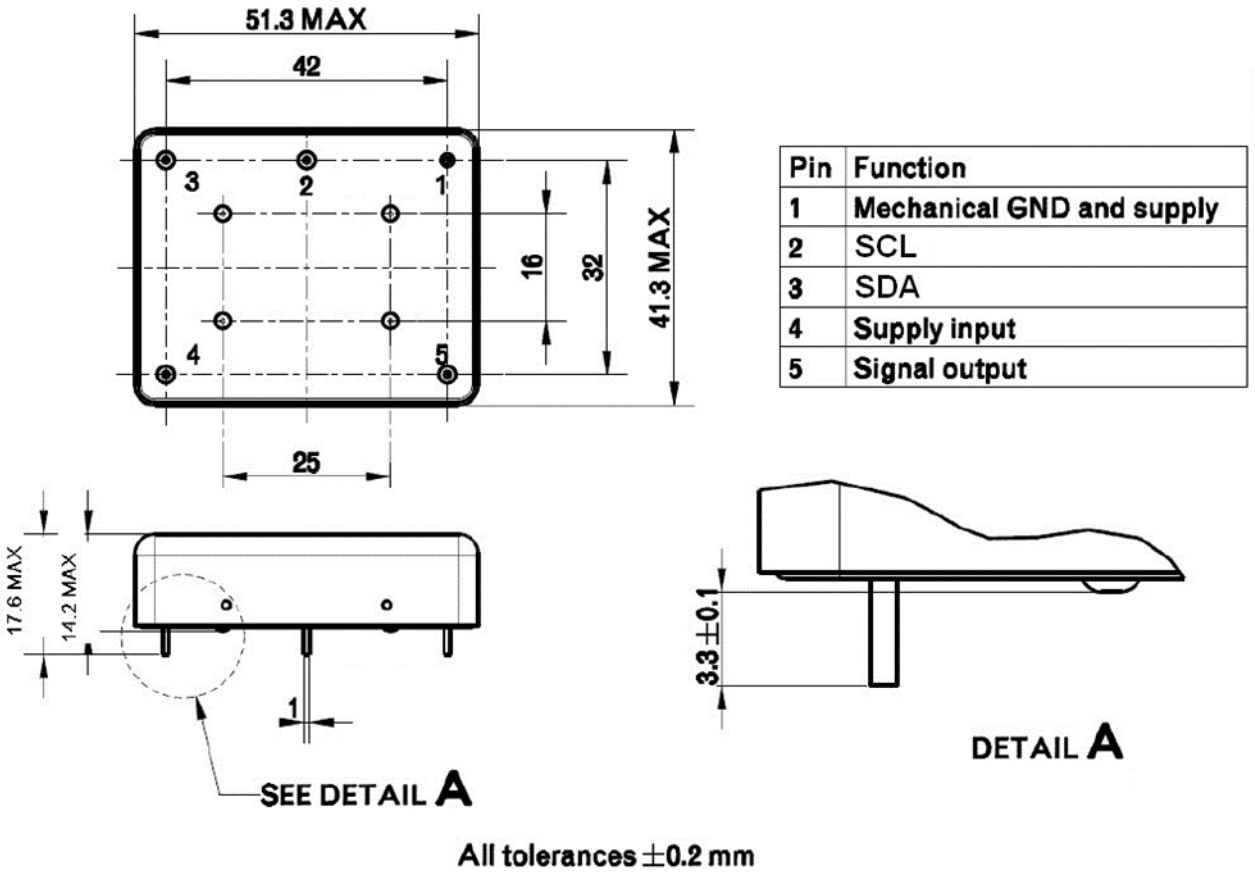
17.0 Disclaimer

Parameter	Description
Disclaimer	"Samples supplied according to this specification are supplied from our development or pre-production programme and as such are not qualification approved products. No condition, warranty or representation regarding quality, suitability, performance, life or continuation of supply is given or implied and Guarantee in clause 6.1 of our standard Conditions of Sale is not applicable. The right is reserved to change the design or specification or cease supply without notice." – RAKON Limited.

18.0 Application Notes

- Application notes:
  - 093186 - RAKON EVK Hardware Installation Guide
  - 093187- RAKON EVK Software User Guide
- Evaluation Kit ref: 516257 (ROX5242T1 / EVK)

19.0 Model outline – ROX5242T1



Pin	Function
1	Mechanical GND and supply
2	SCL
3	SDA
4	Supply input
5	Signal output

20.0 Specification History

Version	User	Changes	Approver	Date (ISO)
Draft	F. Vittrant	Draft datasheet for exchange with customer	D. Thorax	2020-11-03
-			-	
-			-	