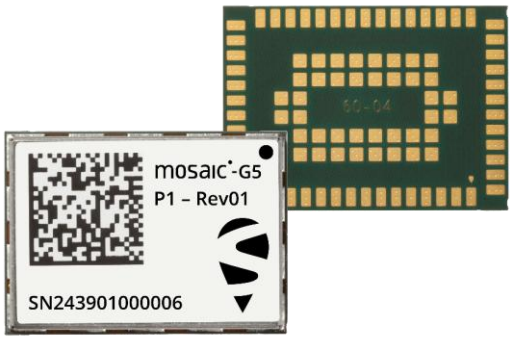
mosaic-G5 Hardware Manual

Version 1.1.1



mosaic-G5 Hardware Manual

Version 1.1.1

May 28, 2025

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Septentrio
Greenhill Campus, Interleuvenlaan 15i
3001 Leuven, Belgium

http://www.septentrio.com
Phone: +32 16 300 800
@Septentrio
https://www.linkedin.com/company/septentrio
https://github.com/septentrio-gnss/
https://www.youtube.com/@SeptentrioGNSS

1 Table of contents

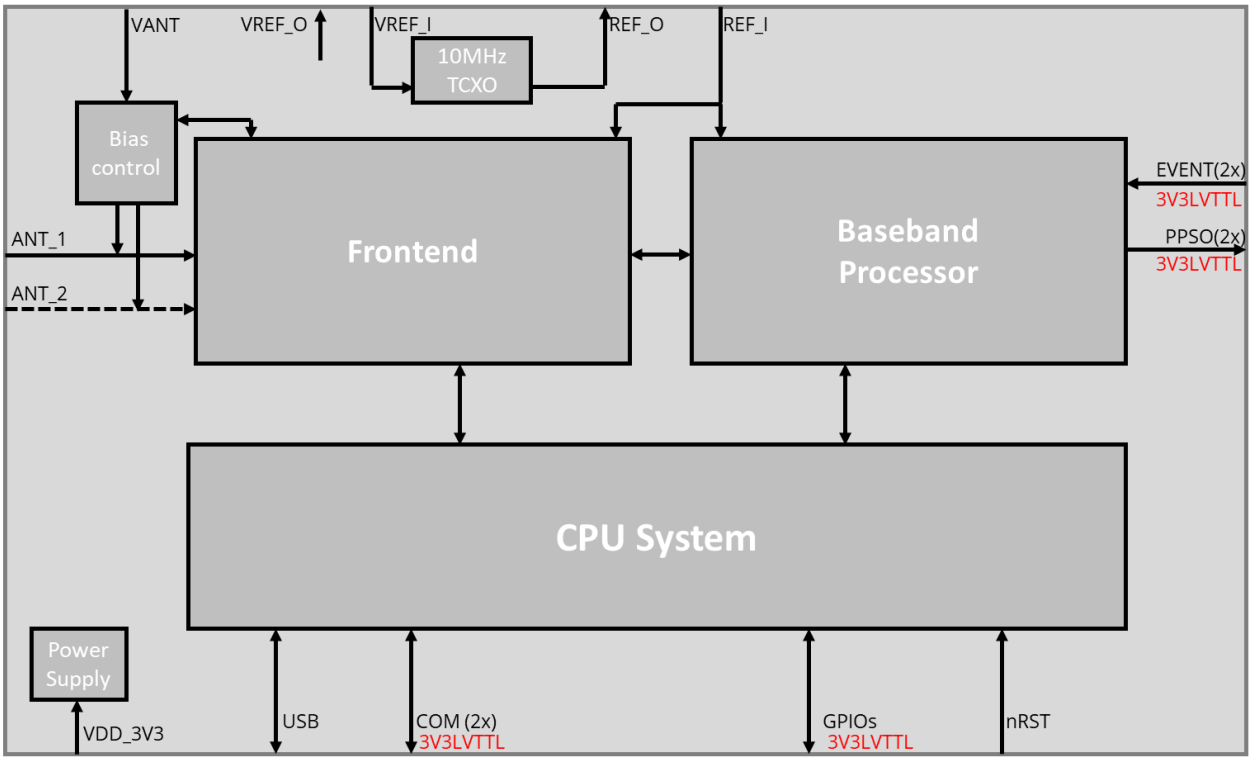
2 Document Change Log

Document Release	Release Date	Main Changes
1.1.0	April 2025	Initial Version
1.1.1	May 2025	Added CE and FCC notices

3 mosaic-G5 GNSS Module

3.1 Overview

Septentrio's mosaic-G5 modules are low-power multi-band multi-constellation GNSS receiver packaged in a 22.8x16.4 mm LGA module. The internal block diagram is shown below.



The module operates from a single 3V3 power supply (VCC).

The ANT_1 input pad receives the RF signal from the main antenna. On dual-antenna modules, a second antenna input is available (ANT_2) for the auxiliary antenna. A 3V to 5.5V DC voltage can be applied to both antennas from the VANT pin, obviating the need for an external antenna supply. The internal bias control circuit detects overcurrent conditions (>150mA) and protects the module in case of short circuit. See section 4.2.

The module can use its internal TCXO as frequency reference, but also optionally accepts an external frequency reference on the REF_I pin. See section 4.5.

Two event timer pins and two PPS outputs are available (3.3V LVTTL). See section 4.6.

The module features the following communication interfaces:

- Two serial ports (3.3V LVTTL), one of them with hardware flow control. See section 4.3.
- USB. See section 4.4.
- GPIOs. See section 4.8.

3.1.1 mosaic-G5 Models and Capabilities

Depending on your mosaic-G5 model, the following features described in this document may not be supported:

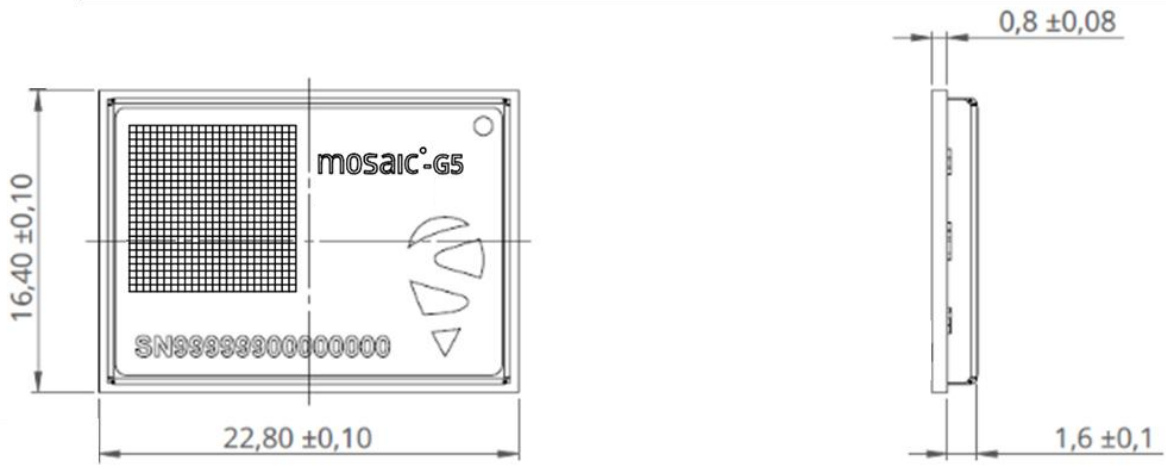
Feature	Available on Models	Section of this Document	Associated Capability
Dual-antenna	P3H	4.2	Antennas / Aux1
10MHz reference input	None (future)	4.5.2	FreqSync
TimeSync input	None (future)	4.6	TimeSync
External event timer	P3, P3H	4.6	TimedEvent

Section “Check the Capabilities of your Receiver” of the mosaic-G5 Reference Guide explains how to check the capabilities of your specific mosaic-G5 module.

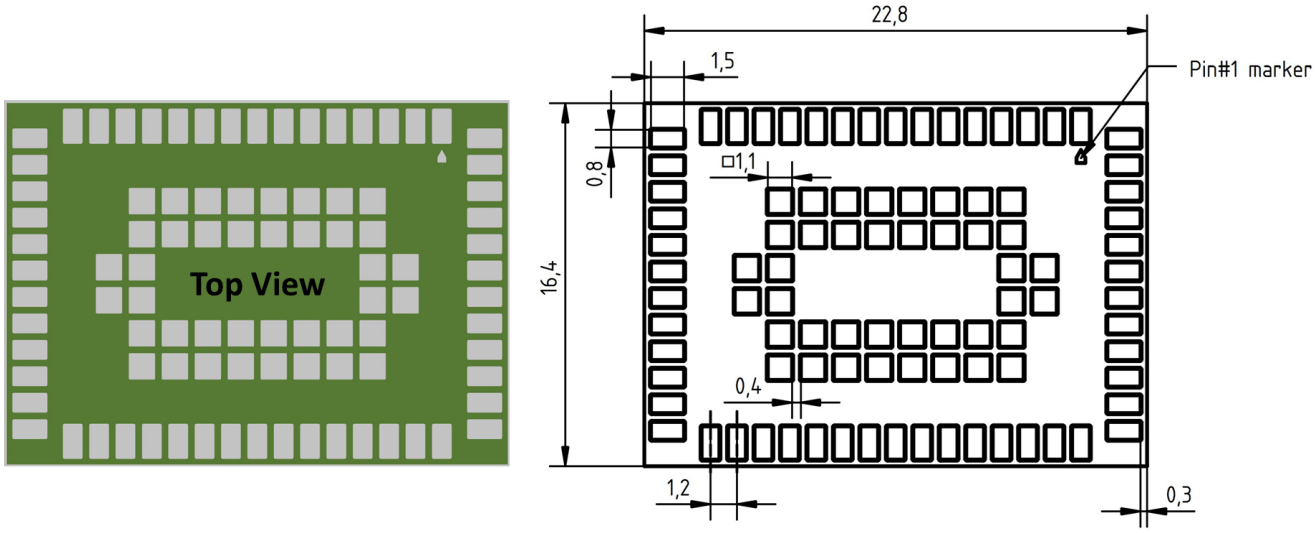
3.1.1.1 Part Numbers

Model	Part Number
mosaic-G5 P1	410461
mosaic-G5 P3	410501
mosaic-G5 P3H	410502

3.2 Mechanical



The hole in the shield marks the position of pin#1.



All dimensions in millimeters.

Weight = 2.2g

3.3 Absolute Maximum Ratings

The following conditions should never be exceeded, even momentarily, as it may cause permanent damage to the module.

Parameter	Comment	Min	Max	Units
VDD_3V3 voltage	See 4.1	-0.3	3.6	V
VANT voltage	See 4.2	-0.3	5.5	V
3V3_LVTTL input pin voltage		-0.3	VDD_3V3+0.3	V
RF input power at ANT_1	See 4.2		20	dBm

RF input power at ANT_2	See 4.2		10	dBm
REF_I level	See 4.5		1.7	Vp-p
Output pins drive current			10	mA
Storage temperature		-55	+85	°C
Operating temperature		-40	+85	°C

3.4 Electrical Characteristics in Operational Conditions

3.4.1 Power Supply

Parameter	Comment	Min	Typ	Max	Units
VDD_3V3 voltage	See 4.1	3.135	3.3	3.465	V
VANT voltage	See 4.2	3.0	3.3	5.5	V
VREF_O output voltage		2.744	2.8	2.856	V
USB_VBUS input current	See 4.4		720		uA
VREF_O output current				50	mA
VANT input current				150	mA

3.4.2 I/O

Parameter	Comment	Min	Typ	Max	Units
VIH, 3.3V inputs		0.7*VDD_3V3		VDD_3V3	V
VIL, 3.3V inputs		0		0.3*VDD_3V3	V
Pull-up, 3.3V inputs[1]	Except nRST_IN	20	40	100	kOhm
Pull-up, nRST_IN		9.6	9.8	10	kOhm
VOH, 3.3V outputs	1 mA	VDD_3V3-0.15			V
VIL, 3.3V outputs	1 mA			0.15	V
REF_I input level		0.8		1.7	Vp-p
REF_I AC input load			5||10		kΩ ||pF
REF_I input frequency			10		MHz
REF_O output level	See 4.5.1		1.2		Vp-p
USB_VBUS voltage	See 4.4	3.0	5.0	5.5	V

3.5 Power Consumption

The module is powered through the VDD_3V3 pins, see section 4.1.

The power consumption primarily depends on which signals are enabled. The following tables list the typical power consumption for some configurations, while tracking all satellites in view from a mid-latitude location, and with the module at room temperature.

[1] The pull-ups are highly non-linear resistors. The listed values represent full swing resistance, applicable when the voltage drop over the pull-up resistors is close to 3V3. Small signal resistance is about 4 times lower.

Single-Antenna:

GNSS Signals	Power (mW)
GPS L1/L2 + GLONASS L1/L2	440
All signals from all GNSS constellations	570
All signals from all GNSS constellations + L-band	670

Dual-Antenna:

GNSS Signals	Power (mW)
GPS L1/L2 + GLONASS L1/L2	600
All signals from all GNSS constellations	785

To account for peak currents, the minimum power supply drive capability should be 500mA.

3.6 Thermal Characteristics

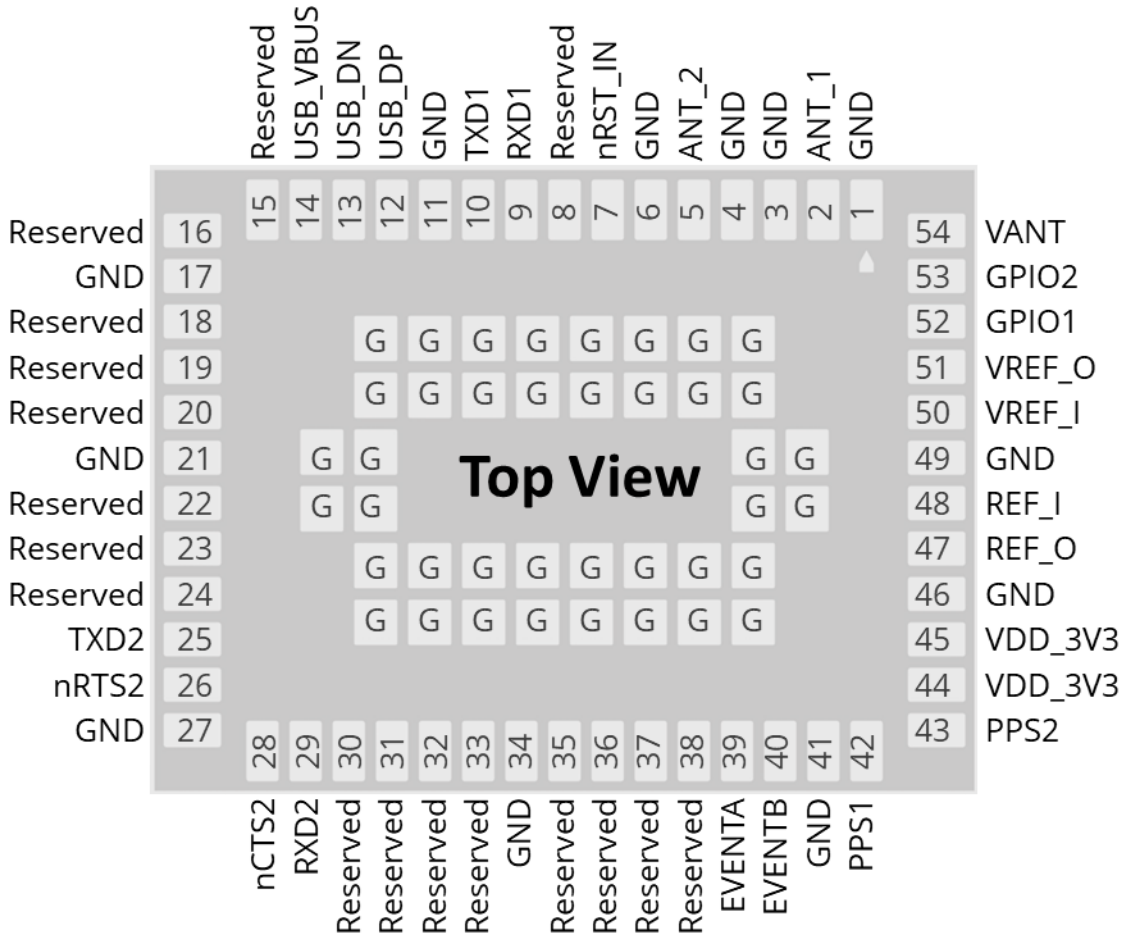
Parameter	Comment	Min	Typ	Max	Units
$\theta_{junction\text{-}case}$			3.2		°C/W
$\theta_{case\text{-}ambient}$	Strongly depends on integration, see footnotes		9[2]	20[3]	°C/W
Operating ambient temperature	Assuming Typ $\theta_{case\text{-}ambient}$	-40		85	°C

[2] 4-layer 6 x 4.5 cm motherboard with one ground layer and copper pours on all other layers, mounted with 4 studs on large metal carrier, natural convection

[3] 4-layer 6 x 4.5 cm motherboard with one ground layer and copper pours on all other layers, mounted on isolating foam, natural convection

4 Pinout and I/O Description

The module provides 54 LGA pads, configured as follows.



The following sections describe all the non-reserved pads.

Conventions:

- Pin Type: I=Input, O=Output, P=Power, Ctrl=Control, Clk=Reference clock
- PU: pulled up
- PD: pulled down
- K: keeper input type

4.1 Power Supply

The module is powered through the VDD_3V3 pins.

Pin Name	Type	Level	Description	Comment
VDD_3V3	P,I	3.3V +/-5%	Main power supply input	Both VDD_3V3 pins must be tied together.
GND	Gnd	0	Ground	All GND pins must be connected to ground.

nRST_IN	Ctrl,PU	3V3_LVTTL	Reset input, active negative. Module is in reset when low.	Internally debounced, can be directly connected to a push-button.

4.2 Antenna(s)

If the Aux1-antenna capability is not available (see section 3.1.1), the module always operates in single-antenna mode. Otherwise, the module can operate in single- or dual-antenna mode. The selection between the modes is done with the **setFrontendMode** user command, as explained in section 4.2.3.

The main antenna must be connected to the ANT_1 pad, and the auxiliary antenna (if applicable) is to be connected to ANT_2.

Both ANT_1 and ANT_2 is ESD-protected (IEC 61000-4-2 class 4) in the module and carry a DC-voltage, avoiding the need for an external bias-tee. This DC-voltage is imposed to the module via the VANT pad. The same voltage is applied to ANT_1 and ANT_2.

The sum of the current drawn by the main and the auxiliary antennas must not exceed 150mA. In case of an overcurrent condition (e.g. short circuit in an antenna cable), the module will first limit the current to about 150 mA and then switch off the ANT_1 and ANT_2 supply after a few milliseconds. It will periodically retry to switch on the antenna supply until the overcurrent condition has disappeared.

Note that the ANT_1 and ANT_2 supplies are always turned off and on together. If an overcurrent is detected on, say, ANT_2, the ANT_1 and ANT_2 supplies will be turned off.

Pin Name	Type	Level	Description	Comment
ANT_1	RF		RF input for main antenna	
ANT_2	RF		RF input for auxiliary antenna	Leave unconnected in single-antenna operation
VANT	P,I	3–5.5V	DC supply to the ANT_1 and ANT_2 antennas. Max current 150mA. DC supply is turned off if overcurrent is detected. If VANT is not connected or if it is tied to GND, there is no DC voltage at the ANT_1 and ANT_2 pads.	

Never inject an external DC voltage into the ANT_1 or ANT_2 pad as it may damage the module. For instance, when using a splitter to distribute the antenna signal to several GNSS receivers, make sure that no more than one output of the splitter passes DC. Use DC-blocks otherwise.

4.2.1 ANT_1 Electrical Specifications

DC bias	DC level provided with the VANT pad
Equivalent DC series impedance at the ANT_1 pin	<= 1 Ohm
Antenna current limit	150 mA (sum of ANT_1 and ANT_2 current < 150mA)
ANT_1 pre-amplification gain range[4]	Single-antenna modules: 15-50 dB (AGC gain: 15-50dB) Dual-antenna modules: 15-35dB (AGC gain: 30-50dB)
ANT_1 receiver noise figure[5] (NFrx, see Appendix B)	8.5 dB with 15 dB net pre-amplification 18 dB with 25 dB net pre-amplification 26 dB with 35 dB net pre-amplification 35 dB with 45 dB net pre-amplification
RF nominal input impedance	50 Ohms
VSWR	< 2:1 in all the supported frequency bands

4.2.2 ANT_2 Electrical Specifications

DC bias	DC level provided with the VANT pad
Equivalent DC series impedance at the ANT_1 pin	<= 1 Ohm
Antenna current limit	150 mA (sum of ANT_1 and ANT_2 current < 150mA)
ANT_2 pre-amplification gain range[4]	15-35 dB (i.e. AGC gain: 30-50dB)
ANT_2 receiver noise figure (NFrx, see Appendix B)	6 dB with 15 dB net pre-amplification 14.5 dB with 25 dB net pre-amplification 21 dB with 35 dB net pre-amplification
RF nominal input impedance	50 Ohms
VSWR	< 2:1 in all the supported frequency bands

[4] The pre-amplification gain is the total gain of the distribution network in front of the module. Typically, this equals antenna active LNA gain minus coax losses in the applicable GNSS bands. The pre-amplification gain can be computed from the AGC gain reported by the module in the `ReceiverStatus` SBF block and shown in the web interface or the RxControl GUI. The conversion formula from the reported AGC gain to the pre-amplification gain is:

Pre-amp gain[dB] = 65 - AGCgain[dB]

So, if the receiver reports an AGC gain of 30dB, the pre-amplification gain is 35dB.

[5] The listed noise figure is at room temperature. It may increase by up to 2 dB at 85°.

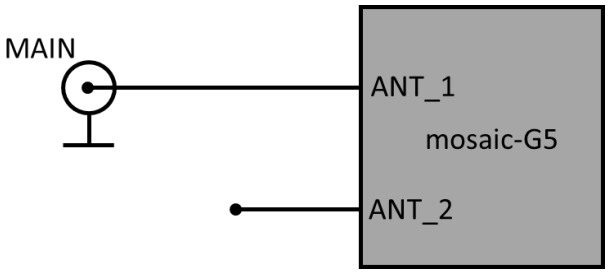
4.2.3 Typical Application

4.2.3.1 Single Antenna Applications

If the Aux1-antenna capability is not available on your module (see 3.1.1), it always operates in single-antenna mode. Otherwise, it can be configured in single-antenna mode by entering the following user commands (needs to be done only once):

- **setFrontendMode, SingleAnt**
  - to configure the module in single-antenna mode at the next reboot
- **exeCopyConfigFile, Current, Boot**
  - to save the configuration in the boot configuration file
- **exeResetReceiver, Hard, none**
  - to reboot

Connect an active antenna to ANT_1. The ANT_1 input is DC-biased and ESD-protected, and an active antenna can directly be connected, without additional components. Make sure to leave the ANT_2 pad open in single-antenna mode.



Refer to 5.4.3 for RF-routing recommendations.

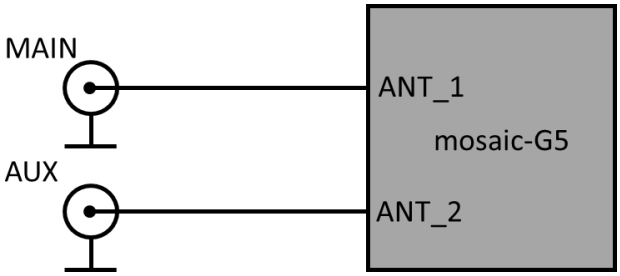
When the module is configured in single-antenna mode, it is recommended to leave the ANT_2 port unconnected. If an antenna is still connected to ANT_2, the warnings in section 4.2.3.2 apply.

4.2.3.2 Dual-Antenna Applications

If the Aux1-antenna capability is available (see 3.1.1), the module can be configured in dual-antenna mode by entering the following user commands (needs to be done only once):

- **setFrontendMode, DualAnt**
  - to configure the module in dual-antenna mode at the next reboot
- **exeCopyConfigFile, Current, Boot**
  - to save the configuration in the boot configuration file
- **exeResetReceiver, Hard, none**
  - to reboot

The main antenna connects to ANT_1 and the auxiliary antenna to ANT_2. Both pads are ESD-protected and are DC-biased. Note that the combined current drawn by both antennas must not exceed 150mA.



Refer to 5.4.3 for RF-routing recommendations.

In dual-antenna mode, the pre-amplification gain must be lower than 35dB on all bands (i.e. AGC gain above 30dB). This may require inserting attenuators in the RF path. See Appendix C for instructions.

In addition, the ANT_1 and ANT_2 pre-amplification must not differ by more than 5dB. It is recommended to use the same antenna type for the main and auxiliary antennas, and, as much as possible, to use antenna cables of the same type and length. In case this is not possible, the strongest signal needs to be attenuated, as also described in Appendix C.

Always connect two antennas when the module is configured in dual-antenna mode. Do not leave ANT_2 unconnected.

4.3 COM Ports

The module provides two serial COM ports. The second one (COM2) supports RTS/CTS hardware flow control:

Pin Name	Type	Level	Description	Comment
TXD1	O	3V3_LVTTL	Serial COM1 transmit line (inactive state is high)	
RXD1	I, PU	3V3_LVTTL	Serial COM1 receive line (inactive state is high)	
TXD2	O	3V3_LVTTL	Serial COM2 transmit line (inactive state is high)	
RXD2	I, PU	3V3_LVTTL	Serial COM2 receive line (inactive state is high)	
nRTS2	O	3V3_LVTTL	Serial COM2 RTS line.	The module drives this pin low when ready to receive data
nCTS2	I, PD	3V3_LVTTL	Serial COM2 CTS line.	Must be driven low when ready to receive data from the module.

Unused COM-port signals can be left floating. Flow control is disabled by default.

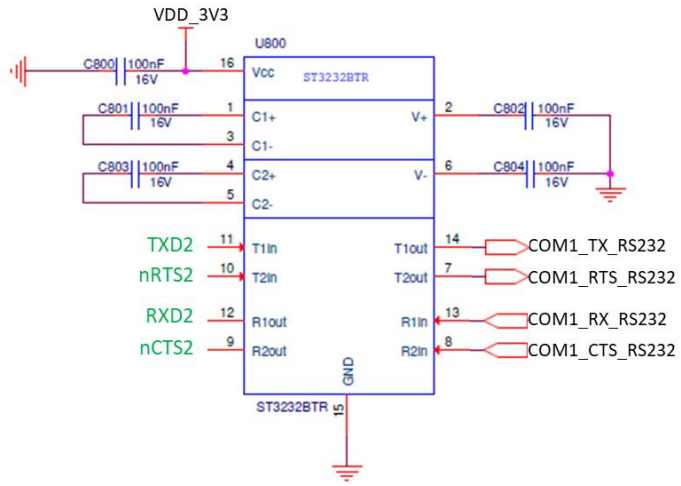
The COM port settings (baud rate, flow control, etc.) are set with the **setCOMSettings** user command (see the Reference Guide for details). The maximum baud rate is 4Mbits/s.

The LVTTL RXD and nCTS inputs of the module shall not be driven while its VDD_3V3 input supply is not present.

4.3.1 Typical Application

An example of a circuit to convert the COM2 signals to RS232 level is shown below. In green, the signals to be connected to the mosaic-G5 pins. The nRTS2 and nCTS2 signals can be left unconnected if hardware flow control is not required.

It is recommended to use the same 3V3 source to supply the RS232 transceiver and the VDD_3V3 pins of the module, to ensure that the transceiver outputs are not driven when the module is not powered.



4.4 USB Device Interface

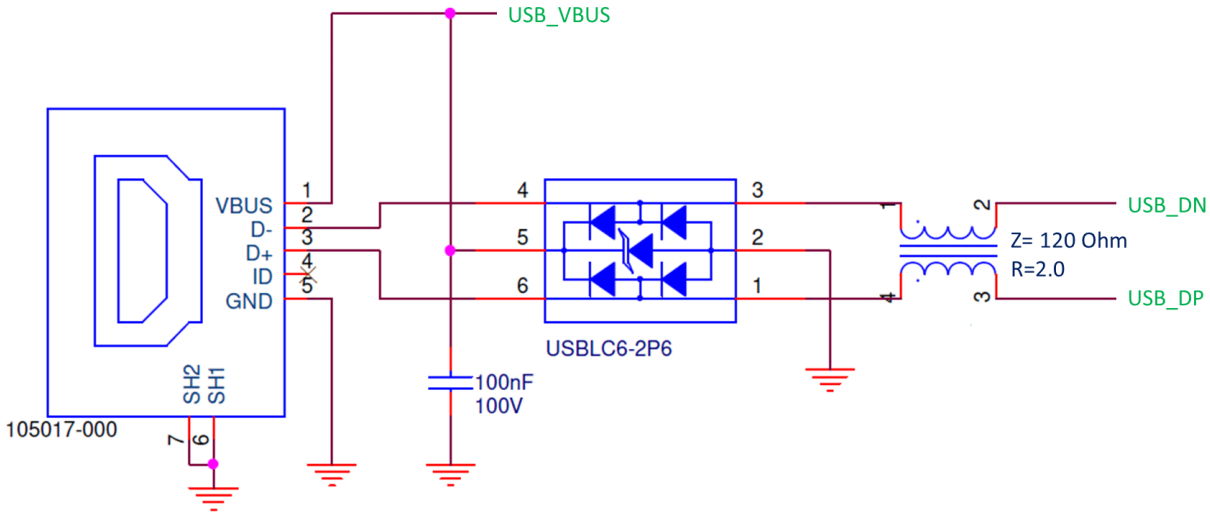
The following pins are used for accessing the module over USB.

Pin Name	Type	Level	Description	Comment
USB_VBUS	P,I	3.00V to 5.5V	USB VBUS input. This pin cannot be used to power the module.	If USB is unused, this pin shall be left floating
USB_DN	I/O	USB	USB data signal, negative	
USB_DP	I/O	USB	USB data signal, positive	

USB is configured to support USB 2.0 mode (high speed, 480Mbps max).

4.4.1 Typical Application

An example of an USB application circuit with ESD protection is shown below. The user shall make sure to use an ESD-protection and common mode choke compatible with high-speed USB if this is desired, for instance the USBLC6-2 from ST and DLP31SN121ML2L from Murata.



4.5 Clock Frequency Reference

The module can use its internal TCXO frequency reference, or can accept an external frequency reference, bypassing the internal TCXO.

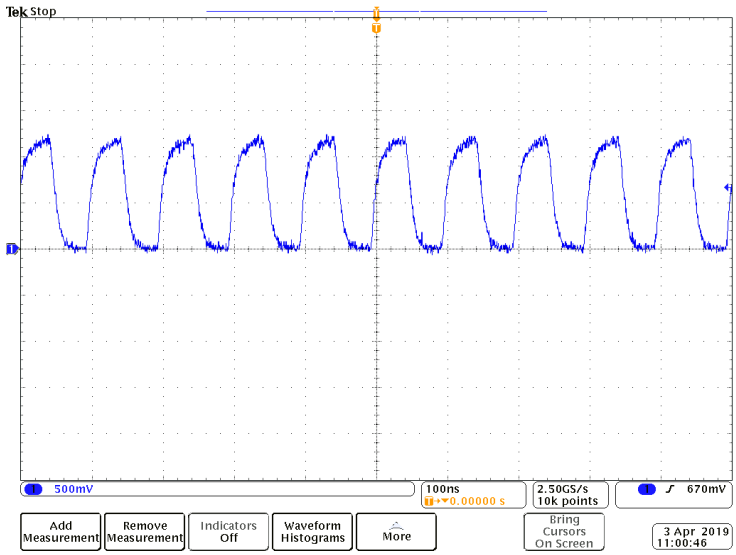
Pin Name	Type	Level	Description	Comment
REF_I	Clk	0.8-1.7Vp-p	Main frequency reference input, DC-decoupled, input impedance is 10 pF // 5 kOhm	See section 4.5.2.
REF_O	Clk	1.2Vp-p	Frequency reference output from the internal TCXO	See section 4.5.1.
VREF_O	P,O	2.8V	2.8V supply output for the internal TCXO.	Do not power any external device from this pin. It is only intended to connect to VREF_I.
VREF_I	P,I	2.8V	2.8V supply input for the internal TCXO. Typically connected to VREF_O.	

4.5.1 Using the internal TCXO

To have the module run on its own TCXO:

- REF_I must be connected to REF_O (those pins are next to each other);
- VREF_I must be connected to VREF_O (those pins are next to each other).

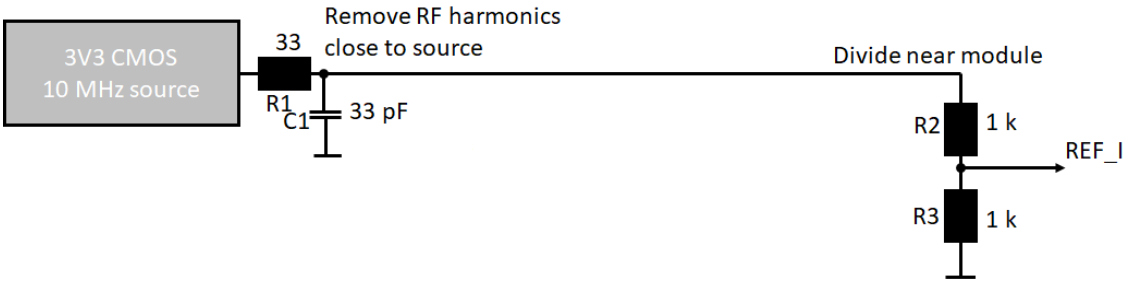
The 10-MHz signal from the internal TCXO is available at the REF_O pin, with peak-to-peak amplitude of 1.2V. The waveform is illustrated in the oscilloscope screen capture below.



4.5.2 Using an external frequency reference

To use an external frequency reference:

- VREF_I must be left unconnected, or be tied to ground.
- REF_O and VREF_O are not used and should be left unconnected.
- The 10-MHz frequency reference must meet the following requirements:
  - Frequency tolerance: +/-2.5ppm
  - Allan variance: better than 1ppb (for tau=1s)
  - Phase noise: better than -90dBc/Hz at an offset of 10Hz
- The 10-MHz reference must be fed into the REF_I pin. It is preferably a sine wave or a band-limited square wave. If CMOS or LVTTL signals are used, it is recommended to filter them at the source with an RC filter with a pole near 100 MHz. The level at the REF_I input must be between 0.8 and 1.7 Vp-p. If a higher signalling voltage is divided with a resistive divider, the impedance level shall be sufficiently low to avoid excessive level drop because of the filtering of the divider with the input capacitance of the REF_I input (10 pF // 5 kOhm). Below an example circuit. The module has a build-in DC-decoupling capacitor.



Appendix D provides an example of an external reference detection circuit.

⚠ Support for an external frequency reference is not available in all mosaic-G5 models. It is dependent on the FreqSync capability (see section 3.1.1). Using an external reference on modules that do not have the FreqSync capability will result in empty or absent SBF output messages.

4.6 Event/TimeSync inputs

If this option is enabled (see the TimedEvent capability in section 3.1.1), the module features two event inputs, which can be used to time tag external events with a time resolution of 3ns.

Pin Name	Type	Level	Description	Comment
EVENTA	I, PD	3V3_LVTTL	Event A or TimeSync input.	Leave unconnected if not used
EVENTB	I, PD	3V3_LVTTL	Event B or TimeSync input.	Leave unconnected if not used

Use the **setEventParameters** user command to configure the EVENTx pins (e.g. to set the polarity.

For correct detection, the minimum time between two events on the same EVENTx pin must be at least 5ms, and there must be no more than 20 events in any interval of 100ms, all EVENTx pins considered.

If the TimeSync capability is available in your mosaic model (see section 3.1.1), the event inputs can also be configured as TimeSync source using the **setTimeSyncSource** command. When an event pin is configured as TimeSync source, the mosaic module expects to see a one-pulse-per-second (1PPS) signal on that pin. It will then synchronize its internal time base (i.e. the time at which GNSS measurements are sampled) to that 1PPS signal. TimeSync is typically used in conjunction with FreqSync (see section 4.5.2) to fully synchronize the module internal time base with the time of an external clock.

Note that there is a delay of a few tens of nanoseconds between the PPS pulse at the EVENT pin and the module internal time base. That delay is dependent on the phase difference between the 10 MHz frequency at the REF_I pin and the PPS pulse at the EVENT pin. It is possible to measure this delay by synchronizing the PPS output pulse with the internal time base, with the **setPPSParameters,,,,RxClock** command.

4.7 PPS output

Pin Name	Type	Level	Description	Comment
PPS1	O	3V3_LVTTL	PPS output. Max output current: 8 mA. Polarity and rate user selectable. During start up, this pin is in high-Z mode. See Reference Guide for operating instructions. Default pulse duration: 5ms.	
PPS2	O	3V3_LVTTL	PPS output. Max output current: 8 mA. Polarity and rate user selectable. During start up, this pin is in high-Z mode. See Reference Guide for operating instructions. Default pulse duration: 5ms.	

The polarity, frequency and pulse width can be set with the **setPPSParameters** and **setPPS2Parameters** command. It is also possible to use these pins as general-purpose output.

During module startup, these pins are first in high-Z mode for about 1s. Then they are driven low for another second before being driven to the intended user-selected level about 2s after powering up the module.

4.8 General Purpose Output (GPIOx)

The GPIO1 and GPIO2 pins are general purpose digital inputs or outputs, of which the function (level or LED status indicator) can be programmed with the **setGPIO1Mode** and **setGPIO2Mode** user command.

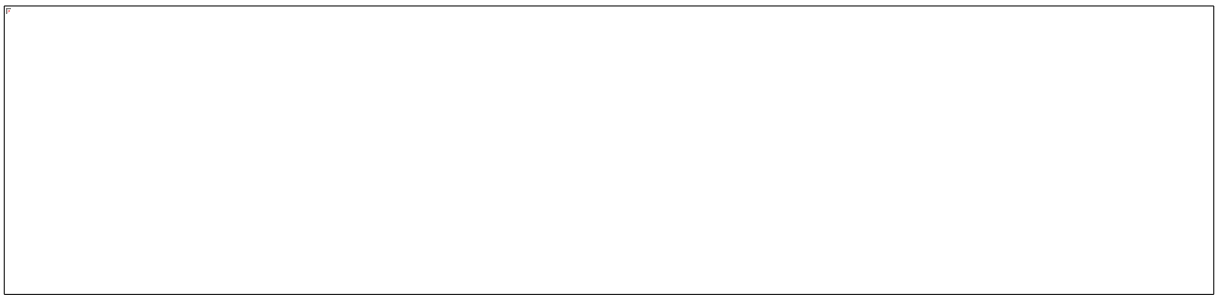
Pin Name	Type	Level	Description	Comment
GPIO1	I/O, PU	3V3_LVTTL	General purpose input/output. Max current in output mode: 16mA	
GPIO2	I/O, PU	3V3_LVTTL	General purpose input/output. Max current in output mode: 16mA	

By default, those pins are configured in input mode with pull-up.

In input mode (GPI), the current electrical level (low or high) is reported in the reply to the **getGPIO1Mode** and **getGPIO2Mode** commands. Note the internal pull-up resistor.

In output mode (GPO), those pins can be set to a solid high or low level, or they can be configured to monitor the module status, in which case they are typically connected to LEDs. An example circuit is shown below, where the LED is wired to light when the GPIO level is low. Refer to the Reference Guide for details.

The module can drive 16mA, so that no external buffer is needed.



During about 2 seconds after powering or resetting the module, these pins are in input mode (pulled up) regardless of the user configuration stored in the boot configuration file.

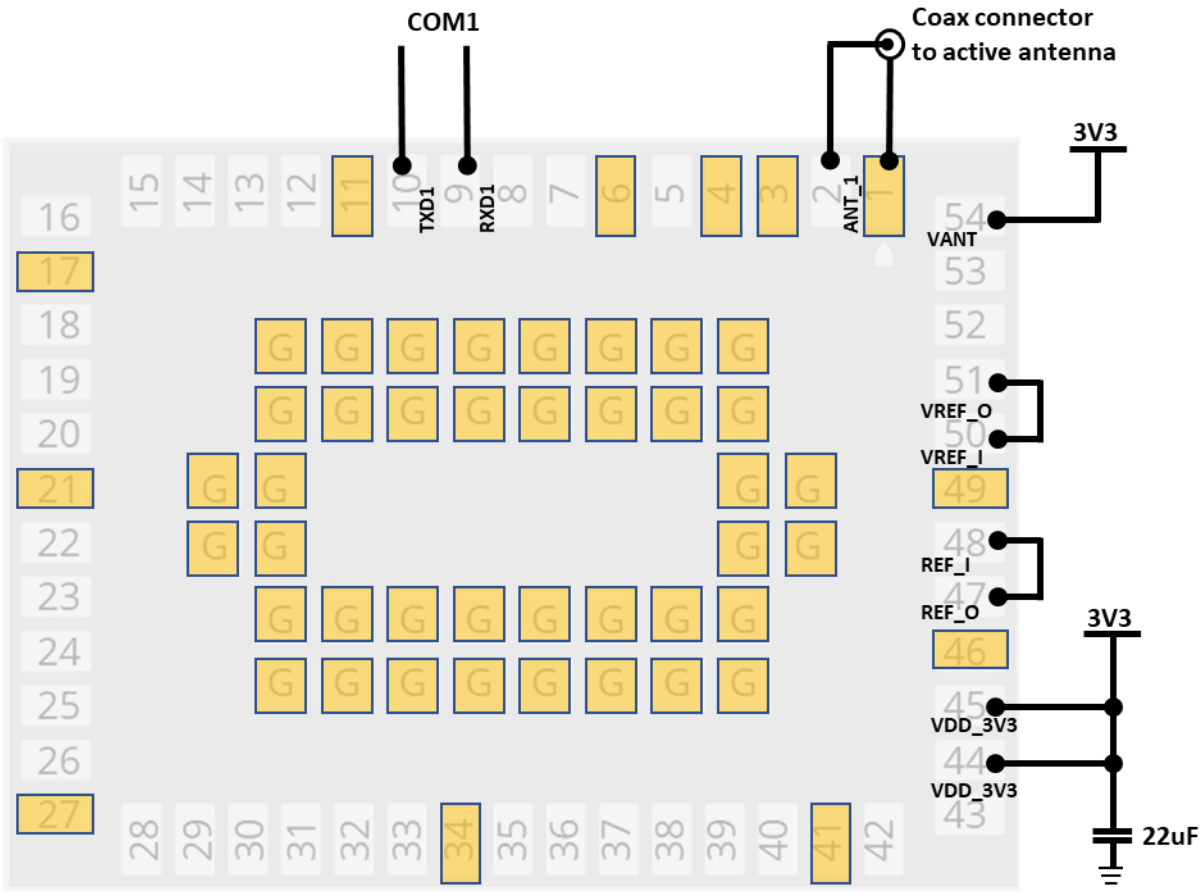
Note that the two PPS output pins (PPS1 and PPS2) can also be configured as general-purpose outputs, but with a maximum current limited to 8mA.

5 mosaic-G5 Integration

5.1 Minimal Design

An example design is shown below:

- All ground pins are connected to ground (pads painted yellow).
- A 3.3VDC supply is provided to the VDD_3V3 pins. A 22µF decoupling capacitor is recommended.
- To provide power to the antenna(s), the VANT pin is also connected to the 3.3V supply.
- The VREF_I and VREF_O pins are tied together, as no external frequency reference is used (see section 4.5).
- The REF_I and REF_O pins are tied together for the same reason.
- The first UART (COM1) is used for communication with the module.
- All other pins are left unconnected.



5.2 Electrical Recommendations

- All ground pins must be connected (pads painted yellow in section 5.1).
- Do not drive a non-zero voltage into input pins (pins type "I" in the tables in chapter 4) when the module is not powered.
- When pull-up/down resistors are needed, use 10 kΩ.
- Unused pins (e.g. pins of an unused interface) must be left unconnected unless explicitly mentioned otherwise.
- Many pins are reserved, which means that their functionality is proprietary or is not supported by the current firmware. Reserved pins must be left unconnected.

5.3 Decoupling

The VDD_3V3 supply shall be decoupled with at least a 22 µF capacitor with proper voltage rating. The other supply terminals don't need external decoupling.

5.4 Layout Recommendations

5.4.1 Coplanarity

It is important to avoid warpage of the motherboard on which the module will be soldered (see section 6.4). More in particular:

- Use a symmetrical layer stack
- Make sure layers opposite from the center of the board have a similar amount of copper (copper-balancing).
- Avoid iron-based soldered shielding cans in the proximity of the module.
- If the motherboard thickness is 1.2 mm or less, it needs to be supported during reflow.

5.4.2 Power

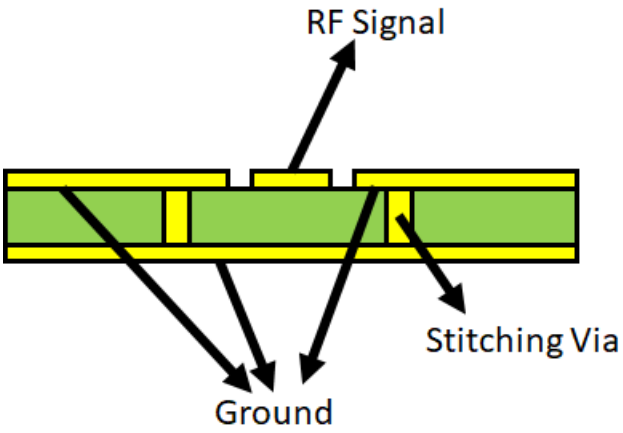
The power trace to the VDD_3V3 terminals should be sufficiently wide to avoid excessive voltage drop. The resistance of the trace to the power supply shall be less than (<minimum supply voltage> - 3.135V)/0.5A.

Use a ground plane.

5.4.3 Antenna Inputs

The antenna input traces shall be routed as a 50-ohm coplanar waveguide with ground, as in the picture below. It is best to use stitching vias every few mm for good ground coherence. The width of the trace to set the impedance to 50 ohm can be calculated with online tools (e.g. https://chemandy.com/calculators/coplanar-waveguide-with-ground-

calculator.htm). Usually, it is best to use the top-layer for the coplanar waveguide and the second layer for ground.



The antenna traces to ANT_1 and ANT_2 can be directly routed to the desired type of coax connector without additional components.

5.4.4 Avoiding Self-Interference

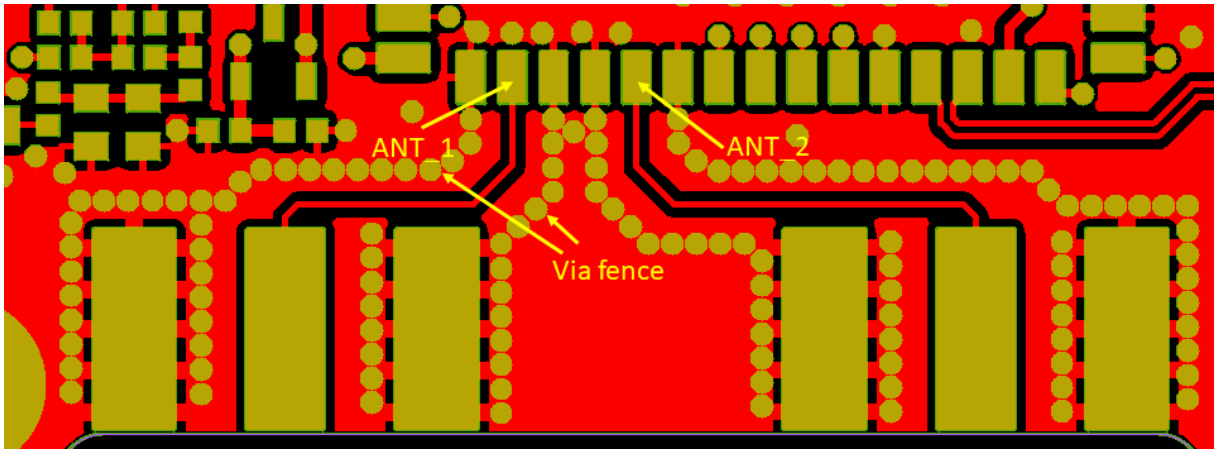
Antenna input connections are sensitive to interference from higher harmonics of other signals on the board. Even clock signals of just a few MHz can produce harmful harmonics at GNSS frequencies (1155-1300 MHz and 1540-1610 MHz).

It is best to keep antenna input traces short, to reduce the area in which signals can be picked up. Stitching vias at the input trace could be arranged as a via fence to shield it from interference.

Furthermore, it is important to avoid digital signals in the MHz-range (SDIO, RMII, MDIO, ...) from running close to antenna inputs.

If a non-sinusoidial external 10-MHz frequency reference is used, high harmonics could interfere with the GNSS signal. This can be avoided by filtering the frequency reference signal with an RC-filter near the source (see section 4.5.2).

In dual antenna designs, both antenna traces shall be isolated from each other by applying a via fence and routing them away from each other as in the example below.



Most self-interference issues relate to radiated interference into a collocated GNSS-antenna. The following applies when the GNSS antenna is closer than 1 meter from electronics which are not in a shielded box:

- High-speed digital signals on the motherboard, like memory busses and clock signals should be routed in an inner layer, flanked with cupper pours connected to ground.

- Large processor and memory chips sometimes already radiate via the bondwires inside their package. Connectors like SD card sockets and radio-module sockets also tend to radiate. It's best to put these components at the side of the board facing away from the collocated antenna. In this way the ground-layer will shield them. Alternatively, they could be placed underneath an EMI shielding can. There is less of a concern if the associated clock frequencies have no harmonics in the GNSS bands.

See also Appendix E.

5.4.5 Thermal Considerations

- Make sure to have at least one full ground plane layer on the motherboard, to transport heat to the mounting points without obstruction. For the other layers, we recommend putting copper pours, connecting them to the ground plane with stitching vias.
- It is recommended to connect all ground pads of the device to a nearby via, to move heat to the ground plane
- Do not put a heat sink on top of the package
- The module was qualified over a -40 to 85°C ambient temperature range with a motherboard compatible with the recommendations above. The chips have significant margin (125°C T_J), but the oscillator will get out of calibration when exceeding the limits, impacting performance.

6 Product Handling

6.1 ESD Precautions

The mosaic-G5 module is compliant with electrostatic discharge (ESD) standard IEC61000-4-2, level 4 (8kV).

It should be manipulated in an ESD-safe environment and using ESD-safe tools and equipment. These tools are typically marked with the following symbol:

The mosaic-G5 module should be stored and handled in the original package (preferably).

6.2 CE and FCC Notices

The mosaic-G5 module has been pre-certified as part of the mosaic-go G5 evaluation kit certification for CE and FCC compliance, as detailed in sections 7.6 and 7.7.

It shall however be noted that CE and FCC certification of the end-product is the responsibility of the integrator and requires good EMC practices as discussed in Appendix E.

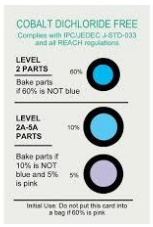
During certification, the highest internal frequency of the module may be requested. This is 3168 MHz.

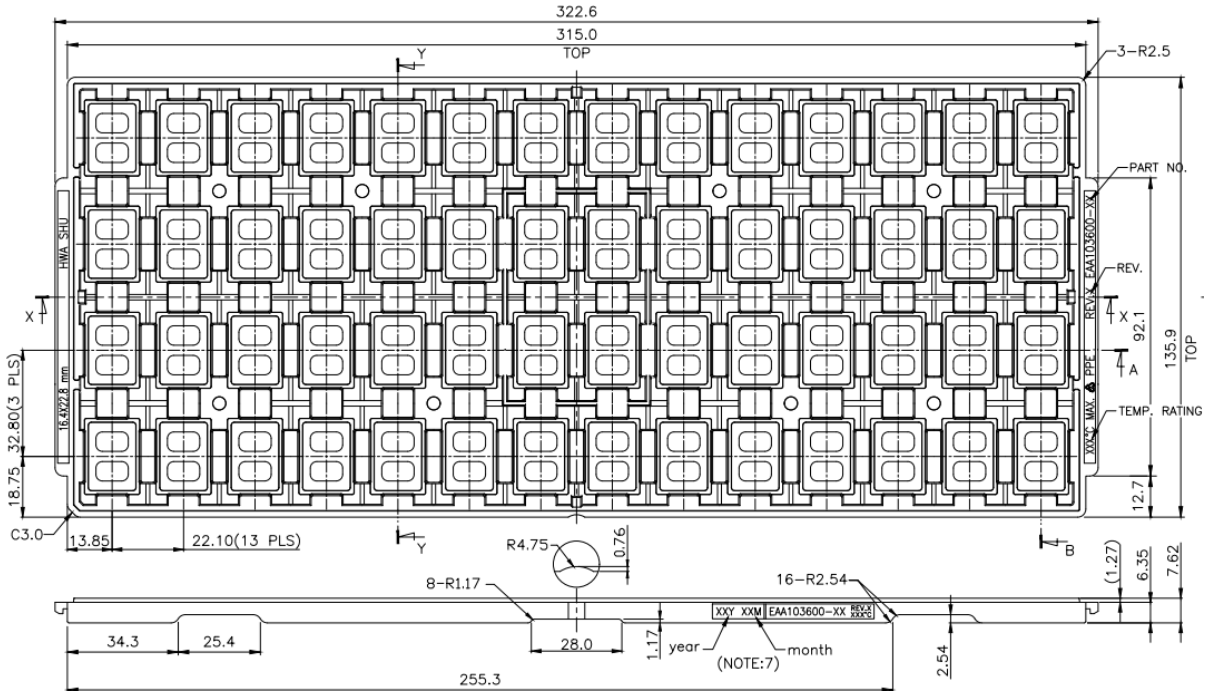
6.3 ROHS/WEEE NOTICE

Septentrio receivers and modules are compliant with the latest WEEE, RoHS and REACH directives. For more info see www.septentrio.com/en/environmental-compliance.

6.4 Packaging

mosaic-G5 modules are delivered on a JEDEC tray in a dry pack, with 56 modules per JEDEC tray.





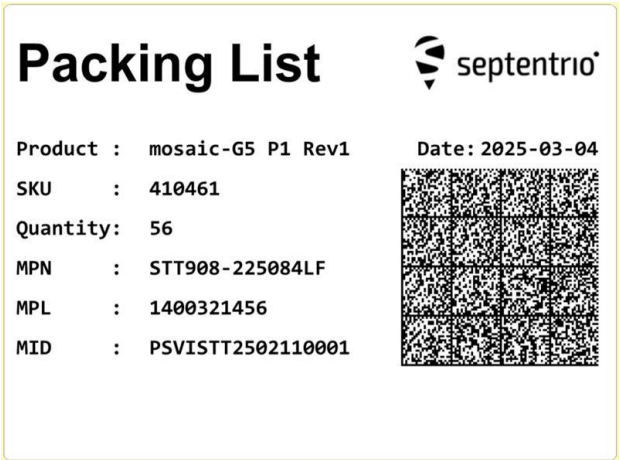
Package contents:

- 56 mosaic-G5 modules
- 1 humidity indicator
- 1 desiccator bag
- Packing list Label
- MSL level label

6.4.1 Packing List Label

The labeling gives product information:

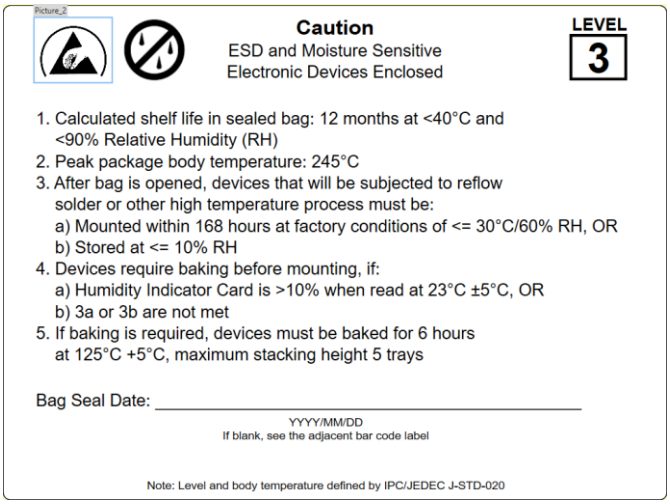
- **Product:** mosaic-G5 variant with hardware revision
- **SKU:** Septentrio Part Number
- **Quantity:** number of modules in the bag
- **MPN:** Manufacturer Part Number
- **MPL:** Manufacturer Product Lot
- **MID:** Manufacturer Packaging ID
- **Date:** Packaging Date
- **Datamatrix:** contains all the Serial Numbers in the package



6.4.2 MSL Level Label

The labeling gives information about:

- Moisture Sensitivity Level and Floor Life
- Storage conditions and baking requirements



6.5 Storage

Dry-pack shelf life is according to JEDEC standard J-STD-033 with 12 months at < 40°C and < 90% relative humidity (RH). After the 12-month period, we recommend checking the packaging condition and HIC status. If required, performed baking prior to reflow on customer boards.

The moisture sensitivity level (MSL) is 3.

If the dry pack has been opened for more than 168 hours or can no longer be considered dry, the modules must be baked. The recommended baking condition is 6 hours at 125°C <= 5% RH.

Oxidation Risk: Baking may cause oxidation and/or intermetallic growth of the terminations, which if excessive can result in solderability problems during board assembly. The cumulative bake time at a temperature greater than 90°C and up to 125°C should not exceed 96 hours.
Bake temperatures higher than 125°C are not allowed.

The 56-position JEDEC tray can sustain baking temperature up to max 150°C. The mosaic-G5 modules can be baked in the JEDEC tray with maximum 5 tray stacked.

6.5.1 Note for Small Quantities

For small quantities requested for prototype usage, Septentrio or Septentrio distributors may not be able to supply the modules in dry-pack packaging. In that case, the customer should consider that the components have exceeded their floor life. To prevent damaging the modules during soldering, they need to be baked prior to any reflow.

6.6 Sticker and Identification

The 2D barcode contains the module variant, hardware version and serial number, e.g:

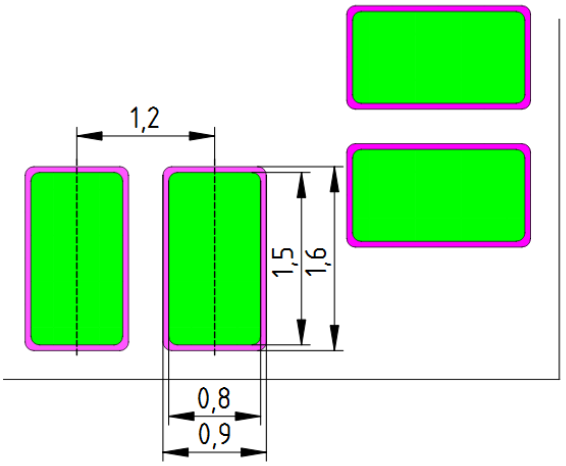
MOSAIC-G5P1GRB00601000AA0401SN24520100001179

The serial number is also printed under the barcode.

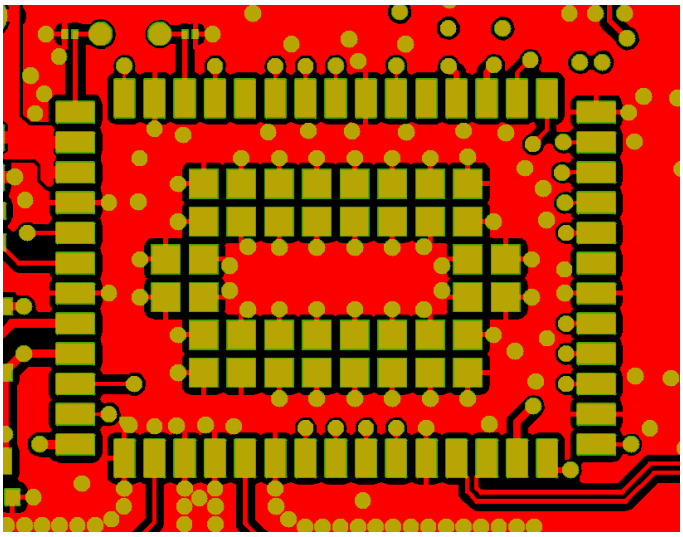
6.7 Soldering

6.7.1 Solder Mask

Non-solder mask defined (NSMD) pads are recommended, with a clearance of 50µm between the copper pad and the solder mask, as shown in the below figure. The copper pads are in green, the (negative) solder mask is in pink. Dimension in millimeters.



The figure below shows an example layout with NSMD pads.



6.7.2 Reflow

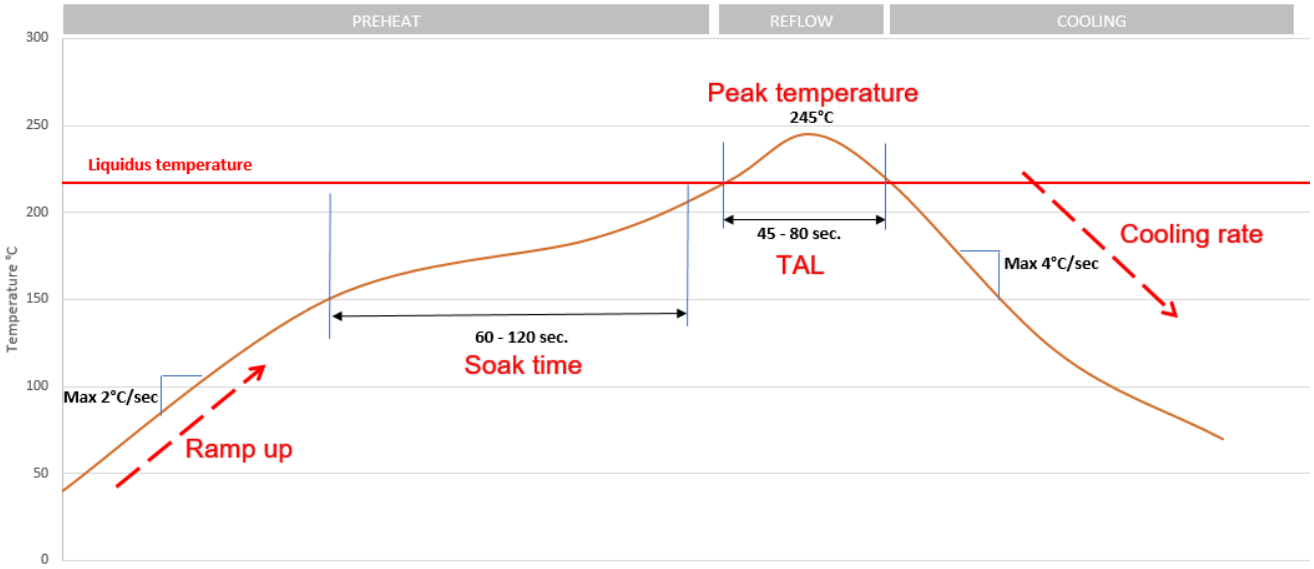
The module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB.

The recommended temperature profile is specified with the graphic below. Refer also to “IPC-7530A: Guidelines for Temperature Profiling for Mass Soldering Processes (Reflow and Wave)”.

The final reflow profile shall be based on Pb-free process and depends on parameters such as the soldering paste, host board parameters (shape, thickness, etc...) and oven capabilities.

Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

To avoid damage to the module, the maximum number of reflows is limited to 2.



Region	Guideline
Ramp up	**max 2 °C/sec**
Soak time	**60-120 sec**
Time Above Liquidus (TAL)	**45-80 sec**
Peak temperature	**245 °C**
Cooling rate	**max 4°C/sec**

Do not use glue underneath the component, as this might lift the component and jeopardize bonding.

The recommended stencil thickness is 0.150 mm (6 mils). The recommended stencil design and thickness may need to be adjusted to meet the specific requirements of assembly processes and product standards.

Mount the part with the largest available placement nozzle, attached to the center of the shield. Use the slowest possible speed of the pick and place machine.
When implemented on a double-sided PCB, the mosaic module must be assembled during the final reflow cycle and cannot be reflowed when located on the bottom side of the board.

If the motherboard thickness is 1.2mm or less, it is recommended to support the assembly during the reflow process to minimize bow of the motherboard.

6.7.3 Cleaning

To ensure the proper functioning and longevity of the module, avoid cleaning with water, solvents, or ultrasonic cleaners. Instead, use a "no-clean" soldering paste to eliminate the need for post-soldering cleaning.

Cleaning with water, solvents or ultrasonic cleaners will void the warranty.

6.7.4 Conformal Coating

Applying conformal coating to this module may impact its performance. The coating material may seep into the module, as the shield does not provide complete protection against low-viscosity liquids. This could lead to signal degradation, reduced sensitivity, or complete failure of the GNSS functionality.

To minimize risks:

- Avoid applying conformal coating directly onto or near the GNSS module.
- Use coatings with appropriate viscosity to prevent infiltration.
- Ensure proper masking and application techniques to protect sensitive components.

Septentrio is not responsible for any performance degradation or device failure resulting from improper conformal coating application.

Conformal coating will void the warranty.

7 mosaic-go G5 Evaluation Kit

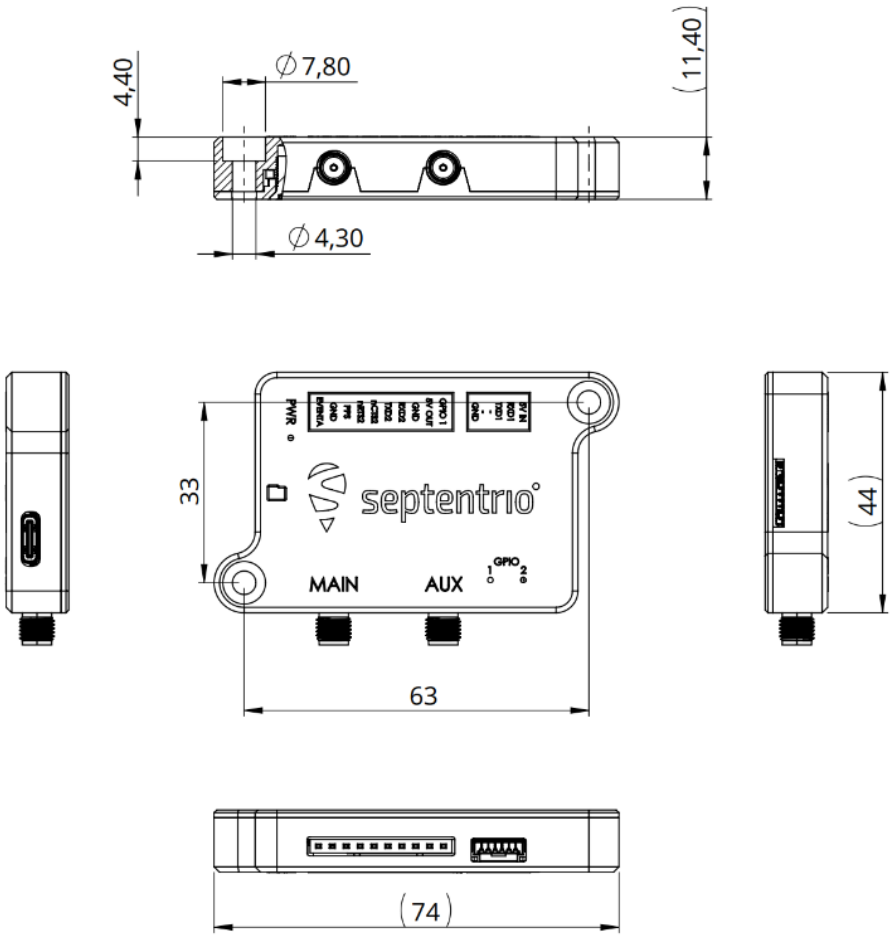
The mosaic-go G5 Evaluation Kit is composed of the mosaic-G5 module soldered on an interface board and protected by an enclosure.

mosaic-go G5 part number:

- mosaic-go G5 P1: **410536** (including accessories).
- mosaic-go G5 P3: **410537** (including accessories).
- mosaic-go G5 P3H: **410538** (including accessories).

The operating and storage temperature range of the mosaic-go G5 Evaluation Kit is -25°C to +85°C.

7.1 Dimensions



All dimensions in mm. Mounting bolt size = M4.

Weight: 50 g

7.2 Connectors

7.2.1 USB

The USB connector is of USB-C type. It is used to control the mosaic-go G5 over USB.

It can also be used to power the mosaic-go G5. See also section 7.4.

7.2.2 MAIN and AUX

These are the main and auxiliary antenna connectors, connected to the ANT_1 and ANT_2 pins of the internal mosaic-G5. See section 4.2 for details.

mosaic-go G5 provides a 5V DC supply to both antenna connectors. The combined main and auxiliary antenna power consumption must not exceed 150mA.

7.2.3 SD Card

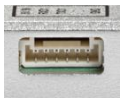
The mosaic-go G5 can log files on the micro-SD Card in this socket. The file system is FAT32, and cards of up to 32GB have been tested.

To reduce the risk of data loss, it is recommended to turn off logging before powering off the mosaic-go G5, by entering the following user command:
setDataInOut,DSK1,,none

Refer to the "Log SBF or NMEA" section of the mosaic-G5 Reference Guide for further instructions.

Note that there is no firmware support to download the files from the card. To read its contents, the card needs to be taken out of the mosaic-go G5.

7.2.4 6-pin JST-GH Connector

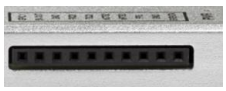


Type: JST_SMB06B, mating connector: JST GHR-06V-S.

Pin Name	Direction	Level	Description	Comment
5VIN	PWR	4.5V-5.5V	Main power supply	
RXD1	In	3V3_LVTTL	Serial COM1 receive line	Direct connection to RXD1 of internal mosaic-G5. See also section 4.3.
TXD1	Out	3V3_LVTTL	Serial COM1 transmit line	Direct connection to TXD1 of internal mosaic-G5. See also section 4.3.
-			Not connected	
-			Not connected	
GND		0	Ground	

All input and output pins are ESD protected.

7.2.5 10-pin 100-mil Socket



Type: standard 10-pin 100-mil 90° socket with gold plating.

Pin Name	Direction	Level	Description	Comment
GPIO1	Out	3V3_LVTTL	General purpose output 1. Max output current: 24mA	This pin exposes the GPIO1 output signal of the mosaic-G5 through a buffer. In mosaic-go G5, the GPIO1 pin can only operate in output mode. See also section 4.8.
5VOUT	Out	5V	5V DC power output Max current: 0.5A	
GND		0	Ground	
RXD2	In, PU	3V3_LVTTL (5V5 tolerant)	Serial COM2 receive line	Connects to RXD2 of internal mosaic-G5. See also section 4.3.
TXD2	Out	3V3_LVTTL	Serial COM2 transmit line	Connects to TXD2 of internal mosaic-G5. See also section 4.3.
CTS2	In, PD	3V3_LVTTL (5V5 tolerant)	Serial COM2 CTS line	Connects to nCTS2 of internal mosaic-G5.

				See also section 4.3.
RTS2	Out	3V3_LVTTL	Serial COM2 RTS line	Connects to nRTS2 of internal mosaic-G5. See also section 4.3.
PPS	Out	3V3_LVTTL		
GND		0	Ground	
EVENTA	In, PD	3V3_LVTTL	EventA input	Connects to EVENTA of mosaic-G5. See 4.6.

All input and output pins are ESD protected.

The pinout order matches the very popular HC-06 Arduino Bluetooth dongles.

The COM port signals (RXD2, TXD2, GND) are compatible with popular USB to 3.3V TTL UART converters such as FTDI's TTL-232R-RPI.

7.3 LEDs

LEDs	Color Component	Short Description
1	Blue	LED lights when level at the GPIO1 pin of the internal module is low. See 4.8.
2	Green	LED lights when level at the GPIO2 pin of the internal module is low. See 4.8.
PWR	Red	LED lights when mosaic-go G5 is powered.

7.4 Powering the mosaic-go G5

There are two ways to power the mosaic-go G5. The nominal input power supply is 5V (4.5V-5.5V range).

- From the USB-C connector. This allows powering the board from a PC or from a standard phone-charger adapter.
- Using the 5VIN pin of the 6-pin connector.

It is safe to connect both supplies at the same time. mosaic-go G5 will use the source with the highest voltage.

Note that the power consumption is about 35% higher than the power consumption of the mosaic-G5 module alone (see section 3.5).

With regards to electrical shock protection, the mosaic-go G5 is an electrical device of class 3, following the definition from IEC 62368-1.

7.5 Accessories

The following accessories are delivered with mosaic-go G5:

Accessory	Part Number	Comment
6-pin COM1 open-ended cable	217729	GH connector in one side and four open ended wires on other side. See wire color code below.
USB cable	217728	USB-C to USB-A cable

7.5.1 6-pin COM1 Open-Ended Cable

Pin name on mosaic-go G5	Wire Color
5VIN	red
RXD1	yellow
TXD1	blue
-	*Not connected*
-	*Not connected*
GND	black

7.6 CE Regulatory Notice

The mosaic-go G5 evaluation kit is in conformity with the relevant European Union harmonization legislation:

- Directive 2014/53/EU – Radio Equipment Directive (RED)
- Directive 2011/65/EU – Restriction of Hazardous Substances (RoHS) Directive incl. amendment (EU)2015/863

The signed Declaration of Conformity (DoC) is available on Septentrio's website (https://www.septentrio.com/en/support/product-resources).

7.7 FCC Regulatory Notice

The mosaic-go G5 evaluation kit complies with Title 47 CFR part 15, subpart B of the FCC rules as a class B device.

Appendix A LED Status Indicators

All GPIO pins can be configured as LED status indicator. See also section 4.8.

The following LED status indicators are supported.

<table>
<tr><th>LED mode</th><th>LED Behaviour</th></tr>
<tr><td>PVTLED</td><td>LED lights when a PVT solution is available.</td></tr>
<tr><td>RTKLED</td><td>LED is off if the PVT is not in RTK mode, blinks in float RTK and is solid on in fixed RTK.</td></tr>
<tr><td>DIFFCORLED</td><td>Differential correction indicator. In rover PVT mode, this LED reports the number of satellites for which differential corrections have been provided in the last received differential correction message (RTCM or CMR).
<table>
<tr><th>LED behaviour</th><th>Number of satellites with corrections</th></tr>
<tr><td>LED is off</td><td>No differential correction message received</td></tr>
<tr><td>blinks fast and continuously (10 times per second)</td><td>0</td></tr>
<tr><td>blinks once, then pauses</td><td>1, 2</td></tr>
<tr><td>blinks twice, then pauses</td><td>3, 4</td></tr>
<tr><td>blinks 3 times, then pauses</td><td>5, 6</td></tr>
<tr><td>blinks 4 times, then pauses</td><td>7, 8</td></tr>
<tr><td>blinks 5 times, then pauses</td><td>9 or more</td></tr>
</table>
If the corrections are received from geostationary satellites over the L-band, the LED will be on for about 1 second, then blink fast twice.</td></tr>
<tr><td>TRACKLED</td><td>
<table>
<tr><th>LED behaviour</th><th>Number of satellites in tracking</th></tr>
<tr><td>blinks fast and continuously (10 times per second)</td><td>0</td></tr>
<tr><td>blinks once, then pauses</td><td>1, 2</td></tr>
<tr><td>blinks twice, then pauses</td><td>3, 4</td></tr>
<tr><td>blinks 3 times, then pauses</td><td>5, 6</td></tr>
<tr><td>blinks 4 times, then pauses</td><td>7, 8</td></tr>
<tr><td>blinks 5 times, then pauses</td><td>9 or more</td></tr>
</table>
</td></tr>
</table>

Appendix B System Noise Figure and C/N0

The system noise figure, in dB, can be calculated as:

$NFsys = 10*\log_{10}(10^{NFant/10} + (10^{NFrx/10}-1)/10^{Gpreamp/10})$

where

- NFant is the antenna LNA noise figure, in dB;
- NFrx is the module noise figure, in dB, as in section 4.2;
- Gpreamp is the net pre-amplification in front of the module, in dB.

For example, with a 2.5-dB antenna LNA noise figure, 30-dB antenna LNA gain and 15-dB cable loss, Gpreamp = 30dB-15dB = 15dB and NRrx is 8.5dB (see table in section 4.2). In this case, the system noise figure is:

$NFsys = 10.\log_{10}(10^{2.5/10}+ (10^{8.5/10}-1)/10^{15/10}) = 2.95$ dB.

The C/N0, in dB-Hz, of a GNSS signal received at a power P can be computed by:

$C/N0 = P - 10.\log_{10}(Tant + 290*(10^{NFsys/10}-1)) + 228.6$ dB

where

- P is the received GNSS signal power including the gain of the antenna passive radiating element, in dBW (e.g. -155dBW)
- Tant is the antenna noise temperature, in Kelvin. Typically Tant = 130K for an open-sky antenna.
- 228.6 is $-10*\log10(k_B)$ with k_B =1.38e-23 J/K the Boltzmann constant.

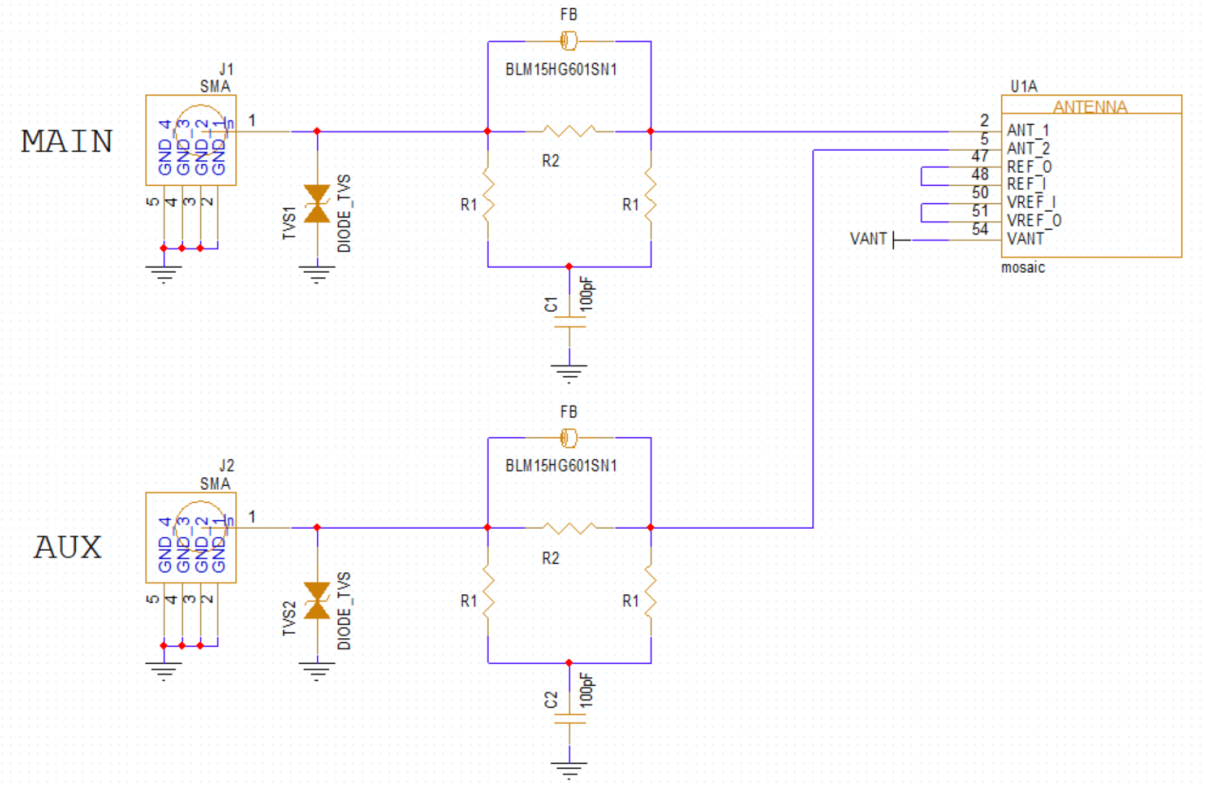
Note that, when connecting the ANT_1 RF input directly to a GNSS simulator, the applicable value for NFsys is 8.5 dB and Tant=290K.

Appendix C Dual-Antenna Gain Adjustment

This appendix in applicable to modules configured in dual-antenna mode with the setFrontendMode user command (see section 4.2).

When operated in dual-antenna mode, the pre-amplification in front of the mosaic-G5 is required to be between 15 and 35 dB (AGC gain reported by the receiver between 30 and 50dB). This is net pre-amplification, equal to the active gain of the antenna minus losses in the coax cables at 1.6 GHz. Above 35 dB of pre-amplification, crosstalk of the auxiliary antenna into the main antenna could degrade performance.

Applications which work with high gain antennas shall use in-line attenuators. These can be implemented on the PCB as indicated in the figure below.



- TVS diode: use SESD0402X1BN-0010-098 or equivalent
- Avoid stubs at the RF path. The components shall be very close to the RF trace and have short grounding if applicable.

If the target attenuation is A dB, the resistors R1 and R2 can be dimensioned as follows, rounding to the nearest E12[6] value:

$$R1 = 50.\frac{1 + 10^{-A/20}}{1 - 10^{-A/20}}\ Ohm$$

$$R2 = \frac{5000.R1}{R1^2 - 2500}\ Ohm$$

The table below shows R1 and R2 values for some common attenuations:

[6] E12 series multipliers of a power of ten: 1.0, 1.2, 1.5, ,1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2

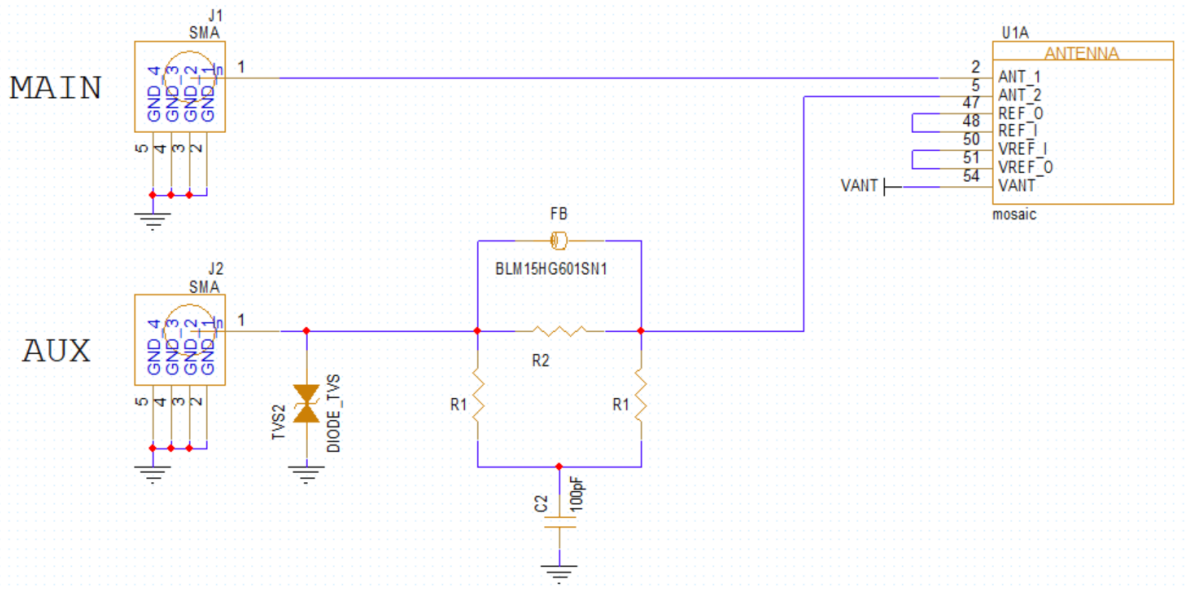
Attenuation [dB]	R1 [Ohm]	R2 [Ohm]
6	150	39
10	100	68
20	56	220

In case a 10-dB attenuator is inserted, the supported net pre-amplification range would be 25-45 dB. If the design is intended for one particular target configuration, for instance with 45 dB pre-amplification, it is recommended to optimize the attenuator towards a 25 dB net pre-amplification in front of the module. In the example of a 45 dB pre-amplification, a 20 dB attenuation shall be targeted.

The difference in pre-amplification in front of the main and auxiliary inputs of the module shall be less than 5 dB. Higher mismatch could induce crosstalk between the signals of both antennas, which could get significant compared to typical errors induced by reflections and antenna non-idealities. When using identical antennas for the main and auxiliary input, differences between pre-amplification usually relate to differences in cable lengths. For example, RG58 cable will typically have between 0.5 and 0.8 dB/m loss at the GNSS operating frequencies (consider 1.6 GHz). Therefore, RG58 cable length differences beyond 6 m could cause issues.

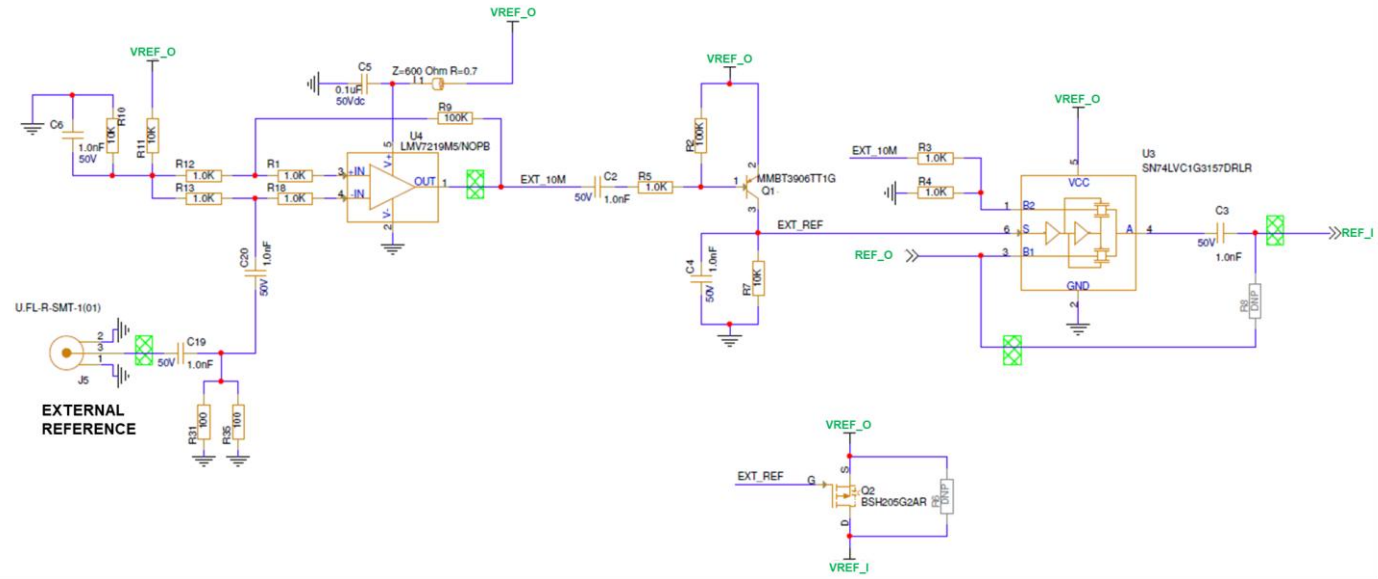
In applications with limited asymmetry between both pre-amplifications (<5 dB), it is recommended to route the stronger signal to the main antenna input and the weaker signal to the auxiliary antenna input of the module.

In applications with a more substantial asymmetry, an attenuator circuit is to be inserted to reduce the strongest signal to the level of the weaker one. An example is shown in the figure below, in which case the strongest signal would be at the AUX connector. R1 and R2 shall be dimensioned as explained earlier, targeting an attenuation equal to the expected difference between the pre-amplifications.



Appendix D Frequency Reference Detection

Section 4.5.2 describes how to use the mosaic-G5 with an external frequency reference. In cases where the external frequency reference is optional, a detection circuit may be useful. An example of such circuit is described here.



The connections to the module are the VREF_I, VREF_O, REF_I and REF_O pins shown in green and described in section 4.5. Note that the signal path includes 1nF capacitors. It is important to use C0G (NP0) types to avoid piezoelectric effects.

With the above circuit, the module uses the external 10-MHz reference provided at the EXTERNAL REFERENCE connector if a suitable signal is detected. In the absence of external reference, the module enables its internal reference. More specifically:

- if there is a valid signal at the EXTERNAL REFERENCE connector (input impedance 50Ω, detection level -14dBm, max supported level +12dBm), EXT_REF is high, VREF_I is floating and the external reference is routed to REF_I through U4 and U3;
- otherwise, EXT_REF is low, VREF_I is connected to VREF_O through Q2 and REF_I is fed with REF_O through U3.

⚠ Switching between external and internal frequency reference must occur when the module is powered off.

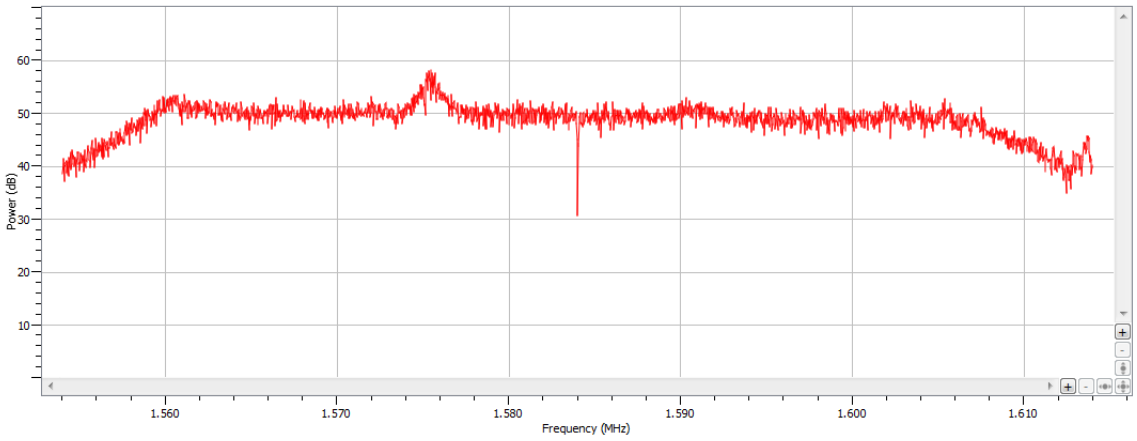
Appendix E EMC Considerations

In applications in which the electronics are collocated with the GNSS antenna, crosstalk could be a major concern. GNSS signals are very weak and easily interfered by radiated harmonics of digital signals.

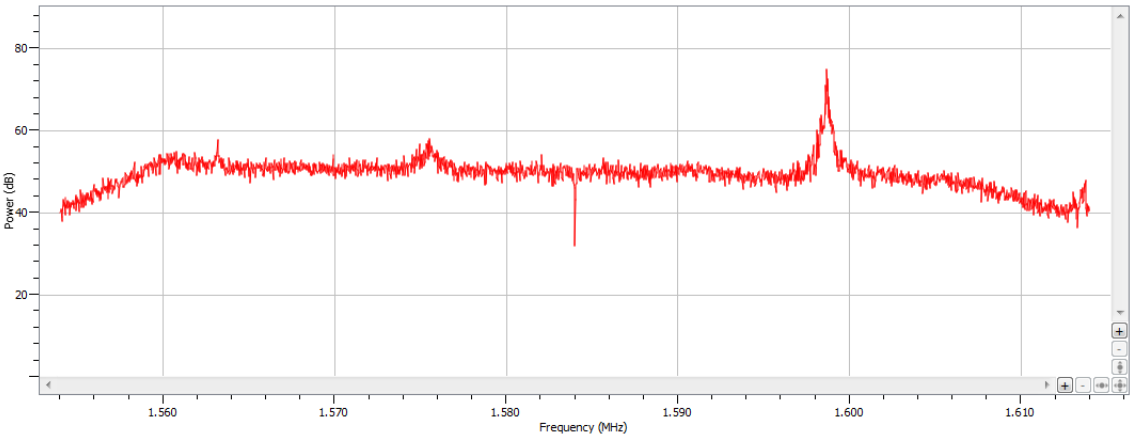
The most useful indicator of the signal reception quality is the C/N0 of the satellites in view. The C/N0 can be viewed in the RxControl graphical interface by clicking *View / Carrier to Noise Plot*. In open-sky conditions, the C/N0 values should reach up to 50 dB-Hz for the strong signals on L1 and L5, and up to 45 dB-Hz on L2, as illustrated below.

If the maximum C/N0 is lower than expected, interference and crosstalk from nearby electronics is likely, and the source of the problem needs to be identified. This is where the RF spectrum monitor built in the GNSS receiver comes in handy. The spectrum monitor can be accessed in RxControl under the *View / Spectrum View* menu. The spectrum can also be monitored offline if the `BBSamples` SBF blocks are logged.

The figure below shows a clean open-sky L1-band spectrum. The bump at 1575MHz corresponds to the GNSS signals at the L1/E1 frequency, and is normal.

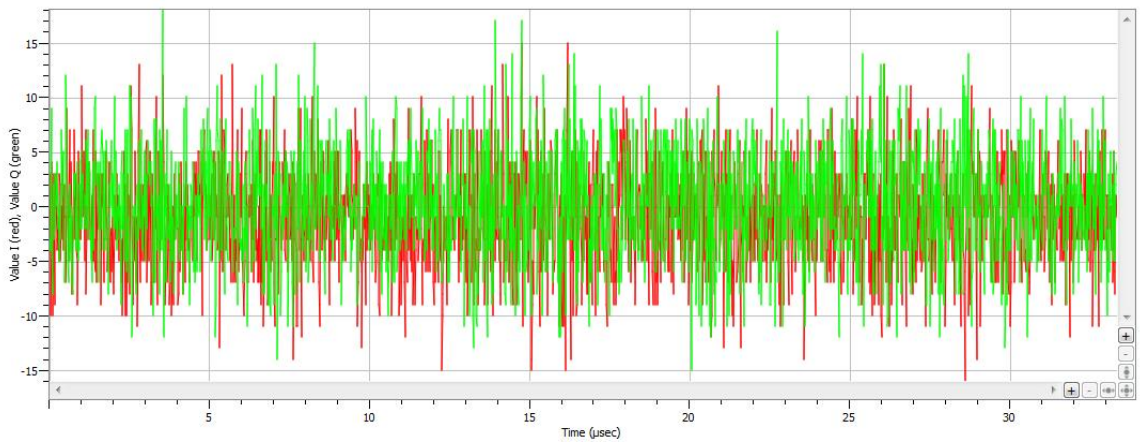


An example of interference is shown below. This particular interference at about 1598 MHz falls in the GLONASS L1 band and slightly degrades the L1 C/N0 of some GLONASS satellites.

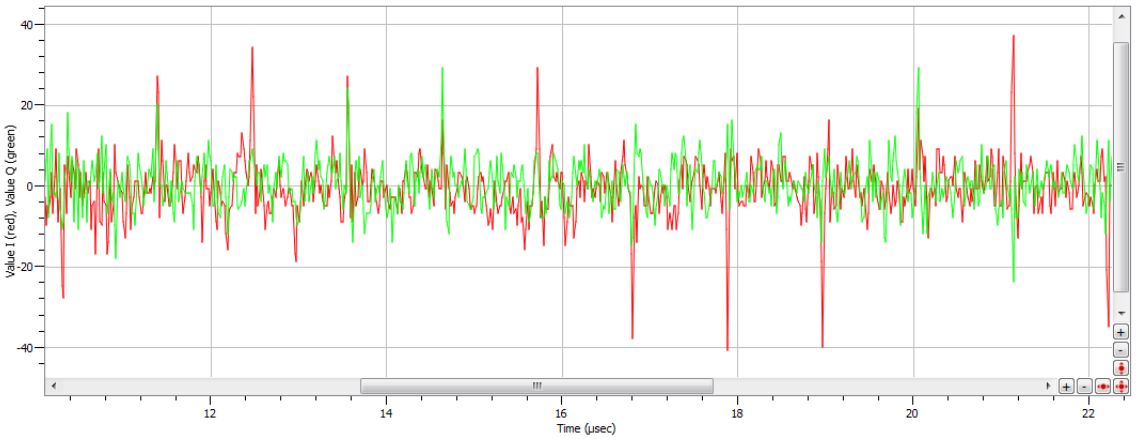


Try to keep personal computers and other equipment more than 2 meters away from the antenna while assessing electromagnetic compatibility of the integration.

RxControl also allows to observe the time domain signal. This should look like white Gaussian noise as illustrated below.



Intermittent interference (µs-scale) has little impact if its duty cycle is below 10%. For example, these short pulses from a digital circuit close to the antenna are essentially harmless.



If interference is detected, look for the root cause by switching off devices. Typical sources of interference are:

- Unshielded flat cables carrying digital signals or power signals towards digital circuits. Particularly, cable joints tend to radiate.
- High-speed digital devices, such as application processors, modems and cameras.
- Digital signals on the application board (e.g. clock signals, SDIO signals).
- Switched-mode power supplies, like buck and boost DC/DC convertors.

If spectral peaks are observed in the spectrum, this usually relates to radiated harmonics. The source can be identified by looking for an integer relation between the observed spectral peaks and the system frequencies. For example, peaks at 1200 and 1248 MHz are an indication of an interfering source at 48 MHz as this maps to the 25th and 26th harmonic of a 48 MHz signal. This may correspond to the frequency of a microcontroller in the application.

Integration crosstalk issues can be prevented or solved in a number of ways:

- Shift the clock frequency of the interfering signal to avoid the GNSS bands.
- Use shielding tape with conductive adhesive.
- Shield radiating circuits, preferably all around.
- Put digital signals in inner layers of the application board.
- For DC/DC convertors:
    - Strictly respect layout guidelines from the manufacturer
    - Avoid burst-mode operation (PFM) when GNSS is active
    - Use synchronous devices
    - Use shielded inductors
- Change the antenna location by experimentation.
- Do not disable the built-in interference mitigation features (see the **setRFInterferenceMitigation** command in the Reference Guide).

The mosaic-G5 module has been designed to minimize radiation and can be used close to an antenna without additional shielding.

It is up to the integrator to ensure EMC regulations of the end-product are met. For this please respect the guidelines of section 5.4.4.