



NEO-D9S-00B

Correction data receiver

Professional grade

Data sheet



Abstract

Technical data sheet describing the u-blox D9 correction data receiver. The module provides global and easy access to satellite L-band GNSS corrections.

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This document applies to the following products:

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NEO-D9S	NEO-D9S-00B-00	PMP 1.04	UBX-22001724 UBX-22039049 UBX-23000084	Mass production

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1 Functional description

1.1 Overview

NEO-D9S-00B is a satellite data receiver for L-band correction broadcast, which can be configured for use with a variety of correction services. It decodes the satellite transmission and outputs a correction stream, enabling a high precision GNSS receiver to reach accuracies down to centimeter level.

1.2 Performance

Parameter	Specification	
Receiver type	NEO-D9S correction data receiver	
L-band satellite		
Specification		
Time to first frame ¹	< 10 s at 2400 bps	
Sensitivity acquisition ²	-133 dBm for BER <10e-5 at 2400 bit/s	
Specification compliance	L-band SESTB28A	
Boot time	<1 s	
Center frequency configuration steps	1 Hz	
Center frequency search window	0 to 65 kHz	
User data rates	600, 1200, 2400, 4800 bps	
Service identifier	Configurable	
De-scrambler	Configurable	
De-scrambling initialization vector	Configurable	
Pre-scrambler	Enable/disable	
Number of concurrent reception channels	1	
UniqueWord	Configurable	
Frequency range	1525 MHz to 1559 MHz	
Communication interface	UART/USB/I2C/SPI	
Communication speed	Up to 921600 baud UART, USB 2.0	
Software backup mode	Available	
Vehicle dynamics	Dynamics	+/- 2g acceleration for all data rates (600 bit/s, 1200 bit/s, 2400 bit/s, 4800 bit/s)
	Velocity	Up to and including 300 km/h

Table 1: NEO-D9S-00B performance

1.3 Supported GNSS augmentation systems

1.3.1 Satellite L-band

The satellite L-band communication system allows GNSS correction service providers to broadcast a variety of services on specific channels, satellites and beams. Consult your service provider on the region their service covers and the specific frequency used. The NEO-D9S-00B must be configured

¹ With respect to an L-band signal using a 20-25 dB external LNA

² Success rate of acquiring an L-band signal > 95% using a 20-25 dB external LNA

according to the specific service as initial identification and decoding of the service provider stream is required.

1.4 Supported protocols

The NEO-D9S-00B supports the following protocols:

Protocol	Type
UBX	Input/output, binary, u-blox proprietary

Table 2: Supported protocols

For specification of the protocols, see the Interface description [2].

2 System description

2.1 Block diagram

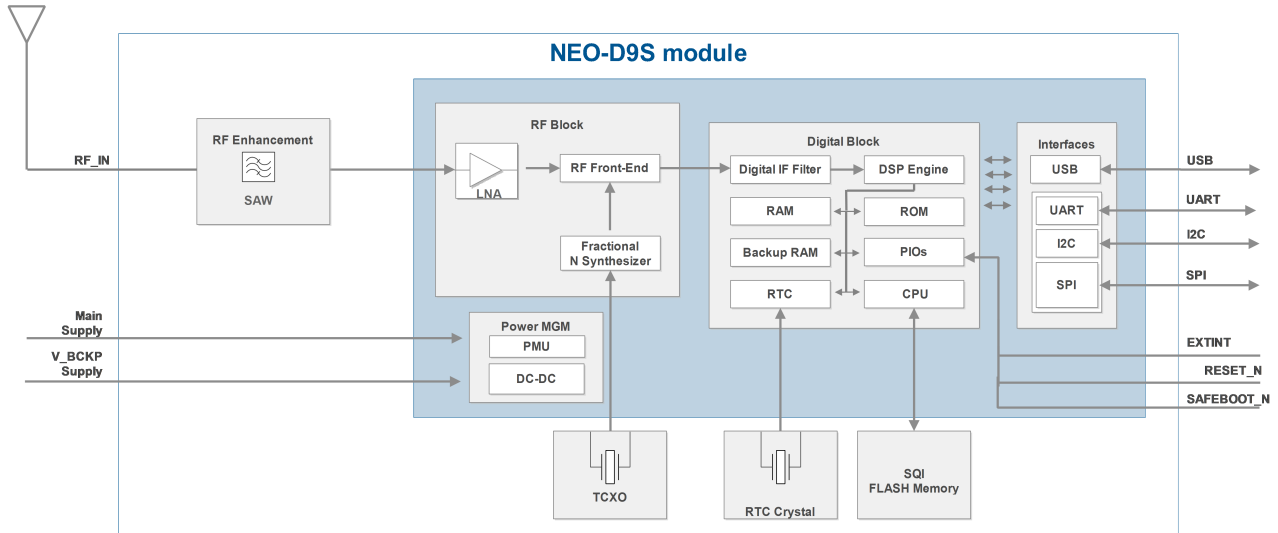


Figure 1: NEO-D9S-00B block diagram

An active antenna is mandatory with the NEO-D9S-00B.

3 Pin definition

3.1 Pin assignment

The pin assignment of the NEO-D9S-00B module is shown in [Figure 2](#). The defined configuration of the PIOs is listed in [Table 3](#).

13	GND	GND	12
14	ANT_OFF	RF_IN	11
15	ANT_DETECT	GND	10
16	ANT_SHORT_N	VCC_RF	9
17	EXTINT	RESET_N	8
NEO-D9S Top View			
18	SDA / SPI CS_N	VDD_USB	7
19	SCL / SPI SLK	USB_DP	6
20	TXD1 / SPI MISO	USB_DM	5
21	RXD1 / SPI MOSI	RXD2	4
22	V_BCKP	TXD2	3
23	VCC	D_SEL	2
24	GND	SAFEBOOT_N	1

Figure 2: NEO-D9S-00B pin assignment

Pin no.	Name	I/O	Description
1	SAFEBOOT_N	I	SAFEBOOT_N (used for FW updates and reconfiguration, leave open)
2	D_SEL	I	UART 1 / SPI select. (open or high = UART 1)
3	TXD2	O	UART 2 TXD
4	RXD2	I	UART 2 RXD
5	USB_DM	I/O	USB data (DM)
6	USB_DP	I/O	USB data (DP)
7	V_USB	I	USB supply
8	RESET_N	I	RESET (active low)
9	VCC_RF	O	External LNA power
10	GND	I	Ground
11	RF_IN	I	Active antenna L-band signal input
12	GND	I	Ground
13	GND	I	Ground
14	ANT_OFF	O	External LNA disable - default active high

Pin no.	Name	I/O	Description
15	ANT_DETECT	I	Active antenna detect - default active high
16	ANT_SHORT_N	O	Active antenna short detect - default active low
17	EXTINT	I	External interrupt pin
18	SDA / SPI CS_N	I/O	I2C data if D_SEL = VCC (or open); SPI chip select if D_SEL = GND
19	SCL / SPI SLK	I/O	I2C clock if D_SEL = VCC (or open); SPI clock if D_SEL = GND
20	TXD / SPI MISO	O	UART1 output if D_SEL = VCC (or open); SPI MISO if D_SEL = GND
21	RXD / SPI MOSI	I	UART1 input if D_SEL = VCC (or open); SPI MOSI if D_SEL = GND
22	V_BCKP	I	Connect to VCC or leave it open
23	VCC	I	Supply voltage
24	GND	I	Ground

Table 3: NEO-D9S-00B pin assignment



For detailed information on the pin functions and characteristics see the integration manual [1].

4 Electrical specification

The limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).



CAUTION Operating the device above one or more of the limiting values may cause permanent damage to the device. The values provided in this chapter are stress ratings. Extended exposure to the values outside the limits may effect the device reliability.



Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum ratings

Parameter	Symbol	Condition	Min	Max	Units
Power supply voltage	VCC		-0.5	3.6	V
Voltage ramp on VCC ³			20	8000	μs/V
Input pin voltage	V _{in}		-0.5	VCC + 0.5	V
VCC_RF output current	ICC_RF			200	mA
Supply voltage USB	V_USB		-0.5	3.6	V
USB signals	USB_DM, USB_DP		-0.5	V_USB + 0.5	V
Input power at RF_IN	Pr _{fin}	source impedance = 50 Ω, continuous wave		10	dBm
Storage temperature	T _{stg}		-40	+85	°C

Table 4: Absolute maximum ratings



CAUTION Risk of equipment damage. This product is not protected against overvoltage or reversed voltages. Use appropriate protection diodes to avoid voltage spikes exceeding the specified boundaries damaging the equipment.

4.2 Operating conditions




The values for the following operating conditions have been specified at 25°C ambient temperature. Extreme operating temperatures can significantly impact the specified values. If an application operates near the min or max temperature limits, ensure the specified values are not exceeded.

Parameter	Symbol	Min	Typical	Max	Units	Condition
Power supply voltage	VCC	2.7	3.0	3.6	V	
SW backup current	I_SWBCKP		0.36		mA	
Input pin voltage range	V _{in}	0		VCC	V	
Digital IO pin low level input voltage	V _{il}			0.4	V	
Digital IO pin high level input voltage	V _{ih}	0.8 * VCC			V	
Digital IO pin low level output voltage	V _{ol}			0.4	V	I _{ol} = 2 mA
Digital IO pin high level output voltage	V _{oh}	VCC - 0.4			V	I _{oh} = 2 mA
DC current through any digital I/O pin (except supplies)	I _{pin}			5	mA	
VCC_RF voltage	VCC_RF		VCC - 0.1		V	
VCC_RF output current	ICC_RF			50	mA	

³ Exceeding the ramp speed may permanently damage the device


Parameter	Symbol	Min	Typical	Max	Units	Condition
Receiver chain noise figure ⁴	NFtot		11		dB	
Recommended LNA gain into module	LNA_gain		20		dB	
Operating temperature	Topr	-40	+25	+85	°C	

Table 5: Operating conditions

 Operation beyond the specified operating conditions can affect the device reliability.

4.3 Indicative power requirements

Table 6 provides examples of typical current requirements when using a cold start command. The given values are total system supply current for a possible application including RF and baseband sections.

 The actual power requirements vary depending on the FW version used, external circuitry, number of satellites tracked, signal strength, type and time of start, duration, and conditions of test.

Symbol	Parameter	Conditions	L - band SESTB28A	Unit
I _{PEAK}	Peak current	Acquisition & tracking	130	mA
I _{AVERAGE}	Average current	Acquisition & tracking	35	mA

Table 6: Currents to calculate the indicative power requirements

All values in **Table 6** are measured at 25 °C ambient temperature.

⁴ Only valid for the L-band band

5 Communications interfaces

The NEO-D9S-00B has several communications interfaces, including UART, SPI, I2C and USB.

All the inputs have internal pull-up resistors in normal operation and can be left open if not used. All the PIOs are supplied by VCC, therefore all the voltage levels of the PIO pins are related to VCC supply voltage.

5.1 UART

The UART interfaces support configurable baud rates. See the Integration manual [1].

Hardware flow control is not supported.

UART1 is the primary host communications interface.

Symbol	Parameter	Min	Max	Unit
R_U	Baud rate	9600	921600	bit/s
Δ_{Tx}	Tx baud rate accuracy	-1%	+1%	-
Δ_{Rx}	Rx baud rate tolerance	-2.5%	+2.5%	-

Table 7: NEO-D9S-00B UART specifications

5.2 SPI

The SPI interface is disabled by default. The SPI interface shares pins with UART and I2C and can be selected by setting D_SEL = 0. The SPI interface can be operated in slave mode only. The maximum transfer rate using SPI is 125 kB/s and the maximum SPI clock frequency is 5.5 MHz.

The SPI timing parameters for slave operation are defined in Figure 3. Default SPI configuration is CPOL = 0 and CPHA = 0.

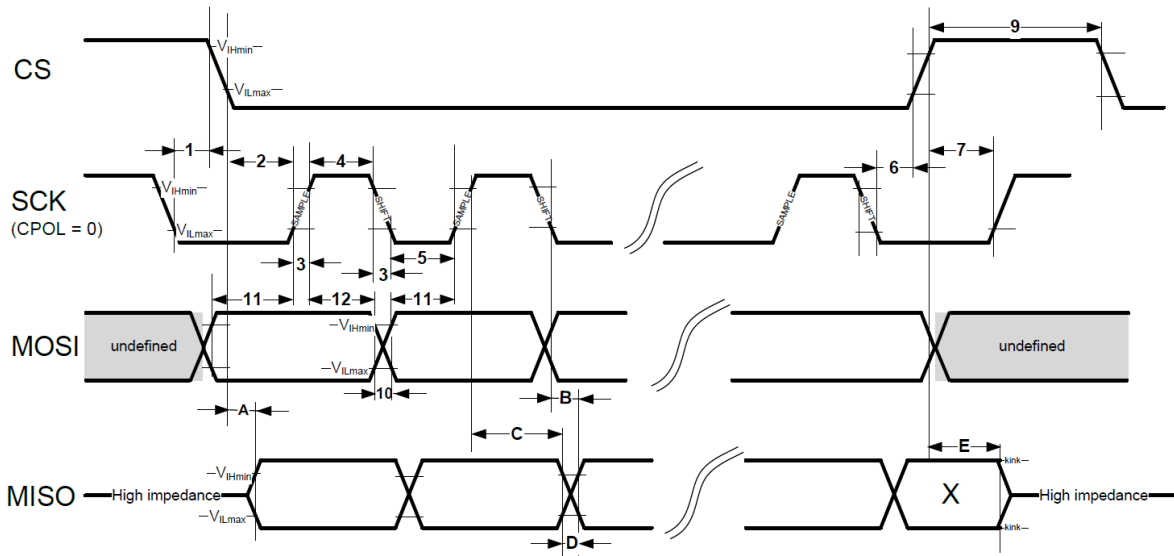


Figure 3: NEO-D9S-00B SPI specification mode 1: CPHA=0 SCK = 5.33 MHz

Symbol	Parameter	Min	Max	Unit
1	CS deassertion hold time	23	-	ns
2	Slave select time (CS to SCK)	20	-	ns

Symbol	Parameter	Min	Max	Unit
3	SCK rise/fall time	-	7	ns
4	SCK high time	24	-	ns
5	SCK low time	24	-	ns
6	Slave deselect time (SCK falling to CS)	30	-	ns
7	Slave deselect time (CS to SCK)	30	-	ns
9	CS high time	32	-	ns
10	MOSI transition time	-	7	ns
11	MOSI setup time	16	-	ns
12	MOSI hold time	24	-	ns

Table 8: SPI slave input timing parameters 1 - 12

Symbol	Parameter	Min	Max	Unit
A	MISO data valid time (CS)	12	40	ns
B	MISO data valid time (SCK), weak driver mode	15	40	ns
C	MISO data hold time	100	140	ns
D	MISO rise/fall time, weak driver mode	0	5	ns
E	MISO data disable lag time	15	35	ns

Table 9: SPI slave timing parameters A - E, 2 pF load capacitance

Symbol	Parameter	Min	Max	Unit
A	MISO data valid time (CS)	16	55	ns
B	MISO data valid time (SCK), weak driver mode	20	55	ns
C	MISO data hold time	100	150	ns
D	MISO rise/fall time, weak driver mode	3	20	ns
E	MISO data disable lag time	15	35	ns

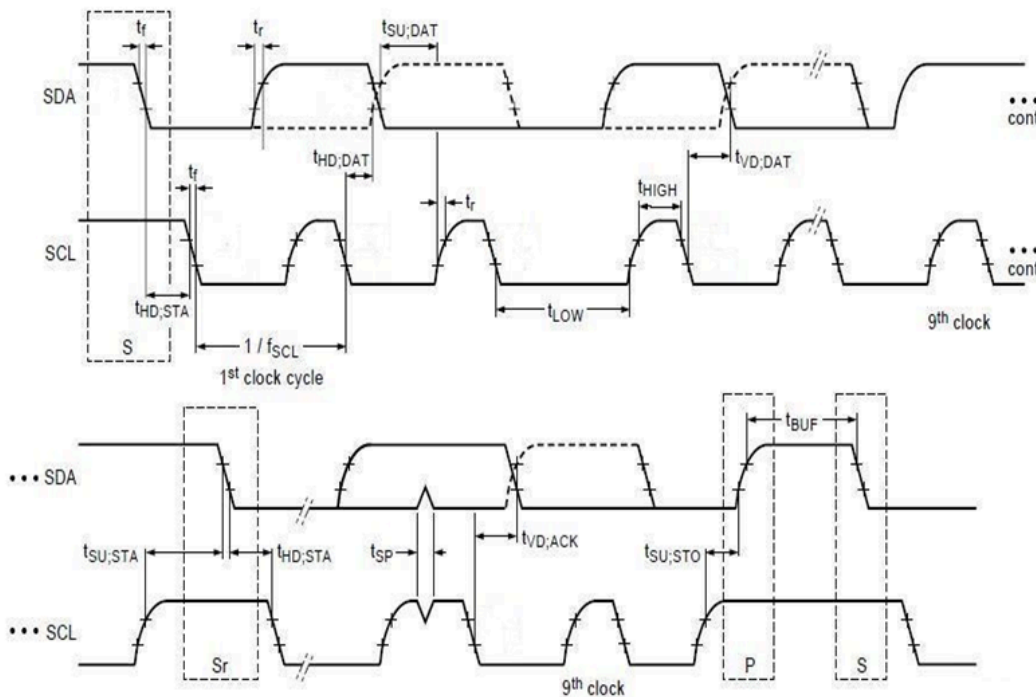
Table 10: SPI slave timing parameters A - E, 20 pF load capacitance

Symbol	Parameter	Min	Max	Unit
A	MISO data valid time (CS)	26	85	ns
B	MISO data valid time (SCK), weak driver mode	30	85	ns
C	MISO data hold time	110	160	ns
D	MISO rise/fall time, weak driver mode	13	45	ns
E	MISO data disable lag time	15	35	ns

Table 11: SPI slave timing parameters A - E, 60 pF load capacitance

5.3 I2C

An I2C interface is available for communication with an external host CPU in I2C Fast-mode. Backwards compatibility with Standard-mode I2C bus operation is not supported. The interface can be operated only in slave mode with a maximum bit rate of 400 kbit/s. The interface can make use of clock stretching by holding the SCL line LOW to pause a transaction. In this case, the bit transfer rate is reduced. The maximum clock stretching time is 20 ms.


Figure 4: NEO-D9S-00B I2C slave specification


Symbol	Parameter	I2C Fast-mode		Unit
		Min	Max	
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.6	-	μs
t_{LOW}	Low period of the SCL clock	1.3	-	μs
t_{HIGH}	High period of the SCL clock	0.6	-	μs
$t_{SU,STA}$	Setup time for a repeated START condition	0.6	-	μs
$t_{HD,DAT}$	Data hold time	0 ⁵	- ⁶	μs
$t_{SU,DAT}$	Data setup time	100 ⁷	-	ns
t_r	Rise time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
t_f	Fall time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
$t_{SU,STO}$	Setup time for STOP condition	0.6	-	μs
t_{BUF}	Bus-free time between a STOP and START condition	1.3	-	μs
$t_{VD,DAT}$	Data valid time	-	0.9 ⁶	μs
$t_{VD,ACK}$	Data valid acknowledge time	-	0.9 ⁶	μs
V_{nL}	Noise margin at the low level	0.1 V_{IO}	-	V
V_{nH}	Noise margin at the high level	0.2 V_{IO}	-	V

Table 12: NEO-D9S-00B I2C slave timings and specifications

⁵ External device must provide a hold time of at least one transition time (max 300 ns) for the SDA signal (with respect to the min V_{ih} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

⁶ The maximum $t_{HD,DAT}$ must be less than the maximum $t_{VD,DAT}$ or $t_{VD,ACK}$ with a maximum of 0.9 μs by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

⁷ When the I2C slave is stretching the clock, the $t_{SU,DAT}$ of the first bit of the next byte is 62.5 ns.

 The I2C interface is only available with the UART default mode. If the SPI interface is selected by using D_SEL = 0, the I2C interface is not available.


5.4 USB

The USB 2.0 FS (full speed, 12 Mbit/s) interface can be used for host communication. Due to the hardware implementation, it may not be possible to certify the USB interface. The V_USB pin supplies the USB interface.

5.5 Default interface settings

Interface	Settings
UART	9600 baud, 8 bits, no parity bit, 1 stop bit. Output protocol: UBX. Input protocols without need of additional configuration: UBX.
USB	Output messages activated as in UART. Input protocols available as in UART.
I2C	Output messages activated as in UART. Input protocols available as in UART.
SPI	Output messages activated as in UART. Input protocols available as in UART.

Table 13: Default interface settings

 The boot message is still output using \$GNTXT messages. The messages are output when the NEO-D9S-00B is powered up.

 Refer to the applicable interface description [2] for information about further settings.

6 Mechanical specification

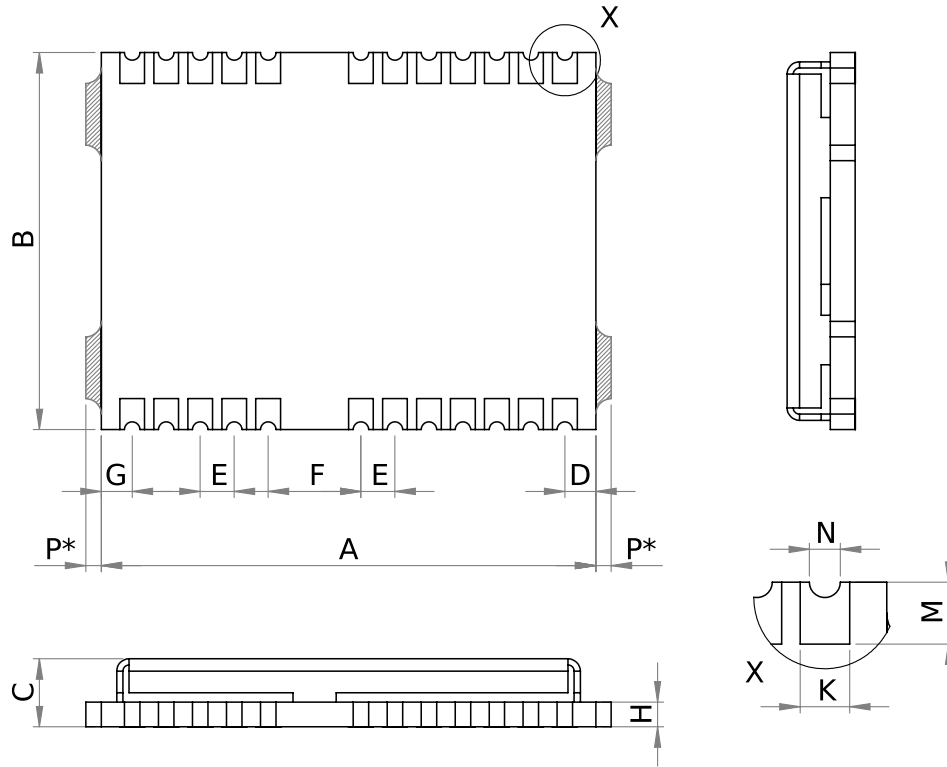




Figure 5: NEO-D9S-00B mechanical drawing

Symbol	Min (mm)	Typical (mm)	Max (mm)	
A	15.9	16.0	16.1	
B	12.1	12.2	12.3	
C	2.2	2.4	2.6	
D	0.9	1.0	1.1	
E	1.0	1.1	1.2	
F	2.9	3.0	3.1	
G	0.9	1.0	1.1	
H	-	0.82	-	
K	0.7	0.8	0.9	
M	0.8	0.9	1.0	
N	0.4	0.5	0.6	
P*	0.0	-	0.5	The de-paneling residual tabs may be on either side (not both).
Weight		1.6 g		

Table 14: NEO-D9S-00B mechanical dimensions

-  The mechanical picture of the de-paneling residual tabs (P*) is an approximate representation, shape and position may vary.
-  Component keep-out area must consider that the de-paneling residual tabs can be on either side (not both).

7 Reliability tests and approvals

NEO-D9S-00B modules are based on AEC-Q100 qualified GNSS chips.

Tests for product family qualifications comply with ISO 16750 "Road vehicles – environmental conditions and testing for electrical and electronic equipment", and appropriate standards.

7.1 Approvals

NEO-D9S-00B complies with the essential requirements and other relevant provisions of the Radio Equipment Directive (RED) 2014/53/EU.

NEO-D9S-00B complies with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

The Declaration of Conformity (DoC) is available on the [u-blox website](#).

8 Labeling and ordering information

This section provides information about product labeling and ordering. For information about moisture sensitivity level (MSL), product handling and soldering see the Integration manual [1].

8.1 Product labeling

The labeling of the NEO-D9S-00B modules provides product information and revision information. For more information contact u-blox sales.

8.2 Explanation of product codes

Three product code formats are used in the NEO-D9S-00B labels. The **Product name** used in documentation such as this data sheet identifies all u-blox products, independent of packaging and quality grade. The **Ordering code** includes options and quality, while the **Type number** includes the hardware and firmware versions.

Table 15 below details these three formats.

Format	Structure	Product code
Product name	PPP-TGV	NEO-D9S
Ordering code	PPP-TGV-NNQ	NEO-D9S-00B
Type number	PPP-TGV-NNQ-XX	NEO-D9S-00B-00

Table 15: Product code formats

The parts of the product code are explained in Table 16.

Code	Meaning	Example
PPP	Product family	NEO
TG	Platform	D9 = u-blox D9
V	Variant	S = L-band corrections
NNQ	Option / Quality grade	NN: Option [00...99] Q: Grade, A = Automotive, B = Professional
XX	Product detail	Describes hardware and firmware versions

Table 16: Part identification code

8.3 Ordering codes

Ordering code	Product	Remark
NEO-D9S-00B	NEO-D9S correction data receiver	u-blox D9 correction data receiver for L-band broadcast

Table 17: Product ordering codes



Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website at: <https://www.u-blox.com/en/product-resources>.

Related documents

- [1] NEO-D9S Integration manual [UBX-19026111](#)
- [2] PMP 1.04 Interface description [UBX-21040023](#)



For regular updates to u-blox documentation and to receive product change notifications please register on our homepage <https://www.u-blox.com>.

Revision history

Revision	Date	Name	Status / comments
R01	26-Mar-2018	jhak	Objective Specification
R02	26-Apr-2019	jhak	Objective Specification
R03	28-June-2019	ghun	Objective Specification - V_BCKP removed
R04	26-Nov-2019	ghun/jhak	Advance Information - V_BCKP pin connect to VCC. I2C, SPI, antenna supervisor, EXTINT, software backup mode added.
R05	05-Feb-2020	ghun/jhak	Early production information - USB added to Absolute maximum ratings table. Vil and Vih updated in Operating conditions table.
R06	27-Oct-2020	dama	USB Interface section update. UART interface section update
R07	24-Jan-2022	dama	Production information - Voltage ramp on VCC value added in Absolute maximum ratings table. V_BCKP general update.
R08	16-Dec-2022	dbhu	Overall text improvement Updated the section Mechanical specification
R09	29-Mar-2023	dbhu	Updated I2C and SPI timing specifications in section Communications interfaces Updated VCC_RF output current in table Absolute maximum ratings

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