mosaic Hardware Manual

Version 1.9.0

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May 24, 2024

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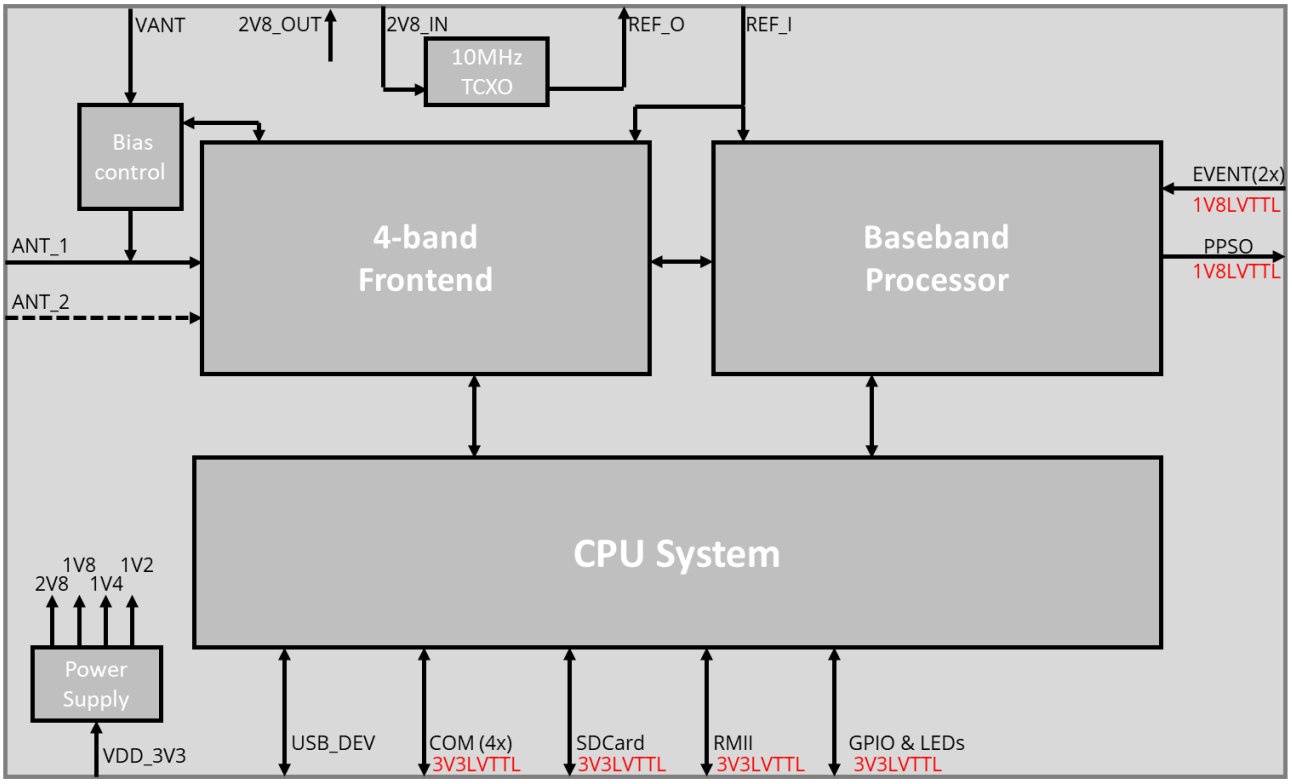
2 Document Change Log

Version	Release Date	Main Changes
1.1.0	Oct 2019	First published version
1.2.0	Jun 2020	Extended the description of the standby mode; Added description of the MODULE_RDY pin; Added power state diagram; Extended and clarified the “Product Handling” section
1.3.0	Jul 2020	Added a note that the RTC_XTALI pin must be tied to ground
1.4.0	Dec 2020	Added description of the dual-antenna mosaic-H; Added complete pad list in appendix
1.5.0	Sep 2021	Added frequency plan in the “Overview” section; Added description of the mosaic-go evaluation kit; Added “mosaic-H RF Gain Adjustment” appendix
1.6.0	Mar 2022	Added documentation of the GPLED2 pin (pin #M3); Added mosaic-CLAS frequency plan
1.7.0	Sep 2022	Extended and clarified the “Product Handling” section (packaging, storage and soldering recommendations)
1.8.0	May 30, 2023	Added dimension tolerances in the “Mechanical” section; Removed references to the deprecated mosaic-Sx model; Updated frequency plan to include the Galileo E6 band in mosaic-X5 and mosaic-T, and to add L-Band support to mosaic-T; Clarified the TimeSync feature; Added an example architecture for a 10-MHz disciplined clock based on mosaic; Added an example of an external 10-MHz detection circuit.
1.9.0	May 2024	Fixed inconsistencies in the naming of the RMII_TXD0 and RMII_TXD1 pins. Made changes to reflect that using an external frequency reference is also possible for mosaic-X5 (previously, it was limited to mosaic-T). Section 4.7.2: added requirements for external frequency reference. Section 6.6.2: increased the recommended stencil thickness to 0.150mm.

3 mosaic GNSS Module

3.1 Overview

Septentrio's mosaic modules are low-power multi-band multi-constellation GNSS receiver packaged in a 31x31mm LGA module. The internal block diagram is shown below.



The module operates from a single 3V3 power supply (VDD_3V3).

The ANT_1 input pad receives the RF signal from the main antenna. On dual-antenna modules (mosaic-H), a second antenna input is available (ANT_2) for the auxiliary antenna. A 3V to 5.5V DC voltage can be applied to the main antenna from the VANT pin, obviating the need for an external antenna supply. The internal bias control circuit detects overcurrent conditions (>150mA) and protects the module in case of short circuit. See section 4.2.

The module can use its internal TCXO as frequency reference, but also optionally accepts an external frequency reference on the REF_I pin. See section 4.7.

Two event timer pins and a PPS output are available (1.8V LVTTL). See section 4.8.

The module features a rich set of communication interfaces:

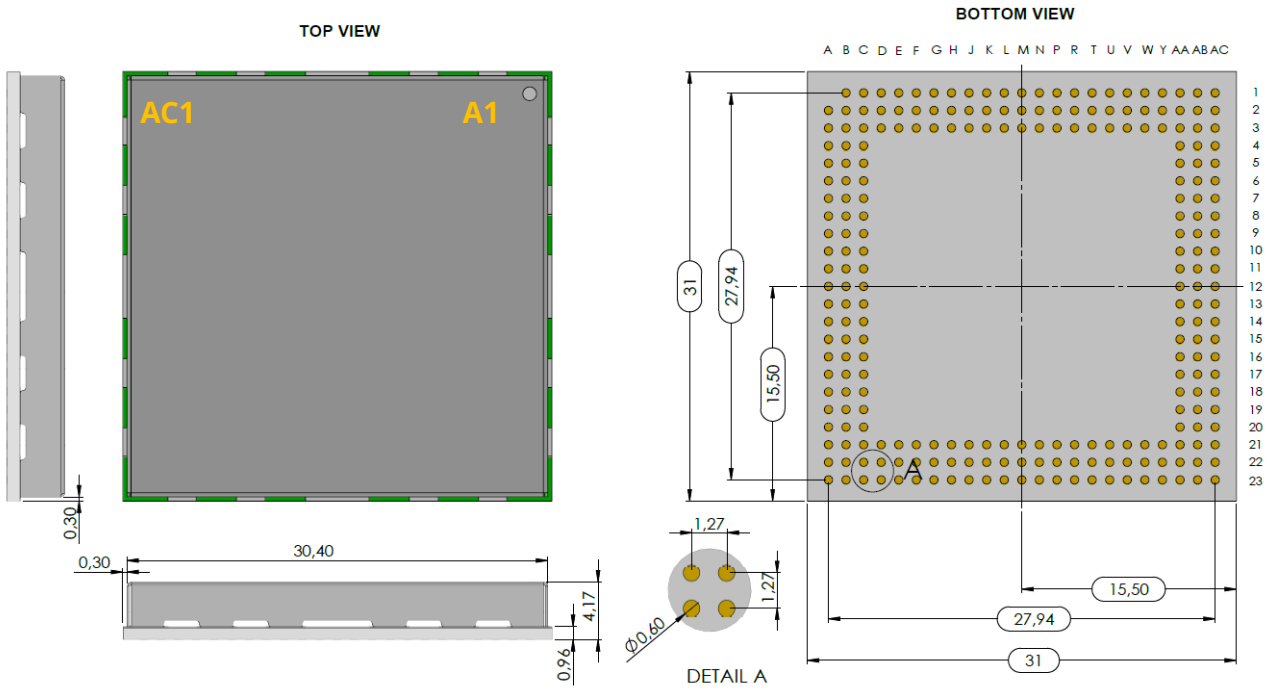
- Four serial ports (3.3V LVTTL), three of them with hardware flow control. See section 4.3.
- USB. See section 4.4.

- Ethernet (the PHY is external to the module). See section 4.5.
- SDCard interface for logging to an external SD card. See section 4.6.
- GPIO and LEDs output. See section 4.11.

The table below summarizes the main differences between the mosaic models in terms of hardware features. The frequency bands in blue are supported.

mosaic model	#Ants	Time & Freq sync	Supported Frequency Bands per Antenna
mosaic-X5	1	Yes	
mosaic-T	1	Yes	
mosaic-CLAS	1	No	
mosaic-H	2	No	mosaic-H can be configured in two different band plans, applicable to both antennas: mosaic-H Band Plan #1:  mosaic-H Band Plan #2:  By default, mosaic-H operates in band plan #1, with the E5b/B2b/B2I band enabled. Band plan #2, with B3 enabled instead of E5b/B2b/B2I, is selected when the BDSB3I signal is enabled with the **setSignalTracking** user command.

3.2 Mechanical



All dimensions in millimeters.

Tolerance:

- PCB dimension: 31x31mm +/- 0.15mm
- Total heigth: 4.17mm +/- 0.3mm

Weight = 6.8g

LGA Details	Specification
Land pitch	1.27 mm
Land diameter	0.6 mm
Pin 1 mark	Bottom: the A1 pad is missing Top: A1 marked by the hole in the shield
Land plating	Nickle/Gold
Array	23 x 23, three outer rows
Number of terminals	239

3.3 Absolute Maximum Ratings

The following conditions should never be exceeded, even momentarily, as it may cause permanent damage to the module.

Parameter	Comment	Min	Max	Units
VDD_3V3 voltage	See 4.1	-0.3	3.6	V
VDD_BAT voltage	See 4.13	-0.3	3.6	V
VANT voltage	See 4.2	-0.3	5.5	V

3V3_LVTTL input pin voltage		-0.3	VDD_3V3+0.3	V
EVENT input voltage	See 4.8	-0.3	1V8_OUT+0.3	V
RF input power at ANT_1	See 4.2		20	dBm
RF input power at ANT_2	See 4.2		10	dBm
REF_I level	See 4.7		1.7	Vp-p
Output pins drive current			10	mA
Storage temperature		-55	+85	°C
Operational temperature		-40	+85	°C

3.4 Electrical Characteristics in Operational Conditions

3.4.1 Power Supply

Parameter	Comment	Min	Typ	Max	Units
VDD_3V3 voltage	See 4.1	3.135	3.3	3.465	V
VDD_BAT voltage	See 4.13	3.135	3.3	3.465	V
VANT voltage	See 4.2	3.0	3.3	5.5	V
USB_VBUS1 voltage	See 4.4	4.4	5.0	5.5	V
1V8_OUT output voltage		1.764	1.8	1.836	V
2V8_OUT output voltage		2.744	2.8	2.856	V
VDD_3V3 current		160	210	500	mA
VDD_BAT input current			0.03	1	mA
USB_VBUS1 input current	See 4.4		10	50	mA
1V8_OUT output current				120	mA
2V8_OUT output current				100	mA
VANT input current				150	mA

3.4.2 I/O

Parameter	Comment	Min	Typ	Max	Units
VIH, 1.8V inputs		0.7*1V8_OUT			V
VIL, 1.8V inputs				0.3*1V8_OUT	V
Input capacitance 1.8V inputs			2.0		pF
Pull-down, 1.8V inputs		80	210	515	kOhm
VOH, 1.8V outputs	7.2 mA	0.75*1V8_OUT			V
VOL, 1.8V outputs	7.2 mA			0.4	V
VIH, 3.3V inputs		0.7*VDD_3V3		VDD_3V3	V
VIL, 3.3V inputs		0		0.3*VDD_3V3	V
Pull-up, 3.3V inputs	Except nRST_IN	68	100	150	kOhm
Pull-up, nRST_IN		9.6	9.8	10	kOhm
VOH, 3.3V outputs	1 mA	VDD_3V3-0.15			V
VIL, 3.3V outputs	1 mA			0.15	V
REF_I input level		0.5		1.7	Vp-p
REF_I input capacitance			8		pF
REF_I input frequency			10		MHz
REF_O output level	See 4.7.1		1.2		Vp-p

3.5 Power Consumption

The module is powered through the VDD_3V3 pins, see section 4.1.

The power consumption depends on the set of GNSS signals enabled and on the positioning mode. The following tables list the average power consumption for some configurations, while tracking all satellites in view from an open sky, and with the module at room temperature. The current is applicable to a supply voltage of 3.3V.

Single-Antenna Modules

GNSS Signals	Positioning Mode	Power (mW)	Current (mA)
GPS L1 C/A	Stand-Alone (1Hz)	550	167
GPS L1/L2	RTK (1Hz)	670	203
GPS/GLONASS L1/L2	RTK (1Hz)	695	211
GPS/GLONASS L1/L2+GALILEO L1/E5a +BeiDou B1C/B2a (phase 3)	RTK (1Hz)	850	258
GPS/GLONASS L1/L2+GALILEO L1/E5a +BeiDou B1C/B2a (phase 3)	RTK (100 Hz)	930	282
GPS/GLONASS L1/L2 + L-band	PPP (1Hz)	760	230
All signals from all GNSS constellations	Static (1Hz)	910	276
All signals from all GNSS constellations +L-band	Static(1Hz)	980	297
All signals from all GNSS constellations +L-band	Static (100Hz)	1080	327

Dual-Antenna Modules

GNSS Signals	Positioning Mode	Power (mW)	Current (mA)
GPS L1 C/A	RTK+heading (10Hz)	680	206
GPS L1/L2	RTK G +heading (10Hz)	900	273
All signals from all GNSS constellations	RTK+heading (10Hz)	1060	321

Enabling wideband interference mitigation with the **setWBIMitigation** command adds 70 mW.

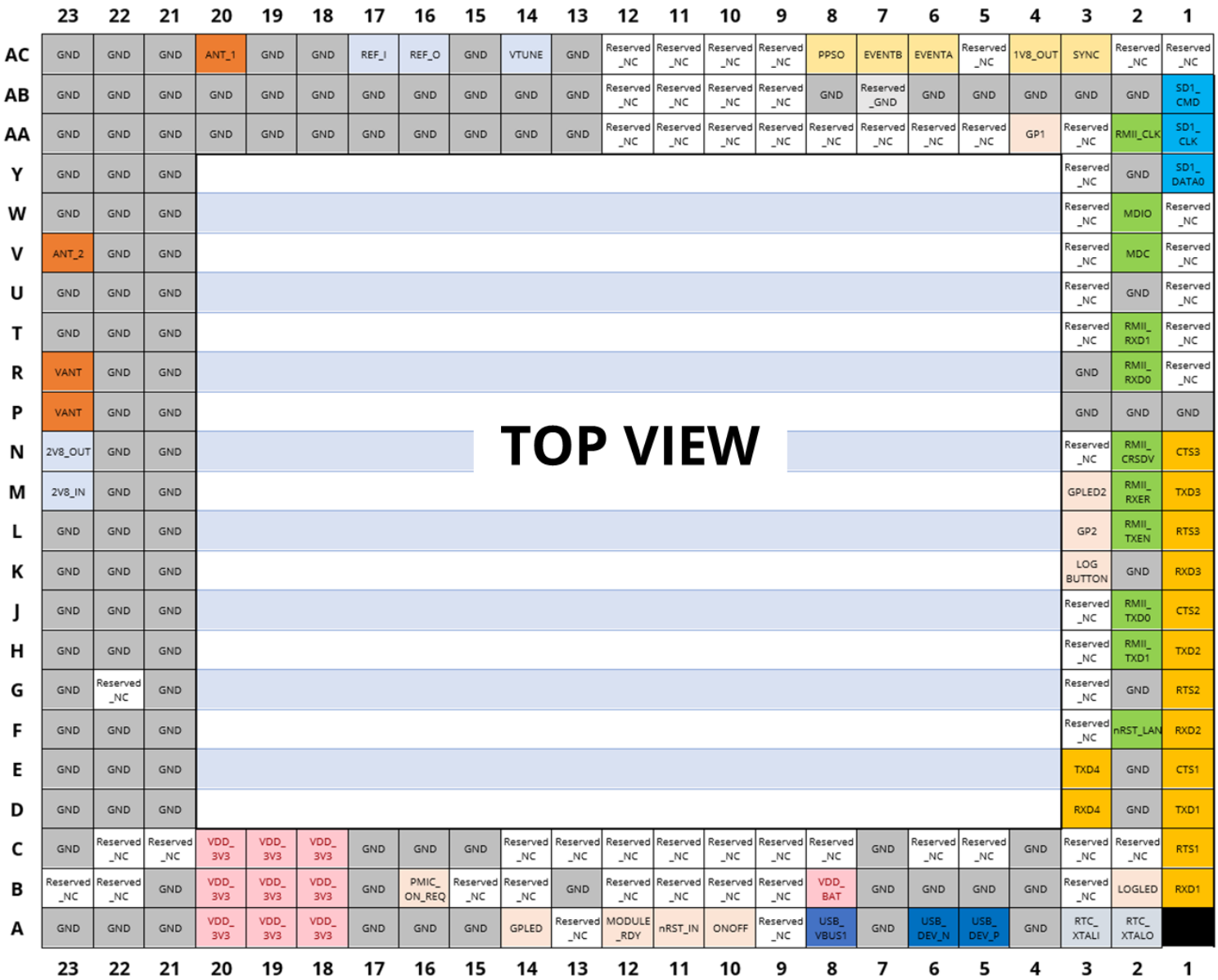
Note that the currents given in the above tables are average values. To account for peak currents, the minimum power supply drive capability should be 500 mA.

3.6 Environmental

Operational: -40 to +85 °C
Storage: -55 to +85 °C

4 Pinout and I/O Description

The module provides 239 LGA pads, configured as follows.



	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AC	GND	GND	GND	ANT_1	GND	GND	REF_I	REF_O	GND	VTUNE	GND	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	PPSO	EVENTB	EVENTA	Reserved _NC	1V8_OUT	SYNC	Reserved _NC	Reserved _NC
AB	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	GND	Reserved _GND	GND	GND	GND	GND	GND	SD1_ CMD
AA	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	GP1	Reserved _NC	RMII_CLK	SD1_ CLK
Y	GND	GND	GND																		Reserved _NC	GND	SD1_ DATA0
W	GND	GND	GND																		Reserved _NC	MDIO	Reserved _NC
V	ANT_2	GND	GND																		Reserved _NC	MDC	Reserved _NC
U	GND	GND	GND																		Reserved _NC	GND	Reserved _NC
T	GND	GND	GND																		Reserved _NC	RMII_ RXD1	Reserved _NC
R	VANT	GND	GND																		GND	RMII_ RXD0	Reserved _NC
P	VANT	GND	GND																		GND	GND	GND
N	2V8_OUT	GND	GND																		Reserved _NC	RMII_ CRSDV	CTS3
M	2V8_IN	GND	GND																		GPLED2	RMII_ RXER	TXD3
L	GND	GND	GND																		GP2	RMII_ TXEN	RTS3
K	GND	GND	GND																		LOG BUTTON	GND	RXD3
J	GND	GND	GND																		Reserved _NC	RMII_ TXD0	CTS2
H	GND	GND	GND																		Reserved _NC	RMII_ TXD1	TXD2
G	GND	Reserved _NC	GND																		Reserved _NC	GND	RTS2
F	GND	GND	GND																		Reserved _NC	nRST_LAN	RXD2
E	GND	GND	GND																		TXD4	GND	CTS1
D	GND	GND	GND																		RXD4	GND	TXD1
C	GND	Reserved _NC	Reserved _NC	VDD_ 3V3	VDD_ 3V3	VDD_ 3V3	GND	GND	GND	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	GND	Reserved _NC	Reserved _NC	GND	Reserved _NC	Reserved _NC	RTS1
B	Reserved _NC	Reserved _NC	GND	VDD_ 3V3	VDD_ 3V3	VDD_ 3V3	GND	PMIC_ ON_REQ	Reserved _NC	Reserved _NC	GND	Reserved _NC	Reserved _NC	Reserved _NC	Reserved _NC	VDD_ BAT	GND	GND	GND	GND	Reserved _NC	LOGLED	RXD1
A	GND	GND	GND	VDD_ 3V3	VDD_ 3V3	VDD_ 3V3	GND	GND	GND	GPLED	Reserved _NC	MODULE _RDY	nRST_IN	ONOFF	Reserved _NC	USB_ VBUS1	GND	USB_ DEV_N	USB_ DEV_P	GND	RTC_ XTALI	RTC_ XTALO	
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

The following sections describe all the non-reserved pads. Pads are grouped by functions. A complete pad list can be found in Appendix G.

Conventions:

- Pin Type: I=Input, O=Output, P=Power, Ctrl=Control, Clk=Reference clock
- PU: pulled up
- PD: pulled down
- K: keeper input type

4.1 Power Supply

The module is powered through the VDD_3V3 pins.

Pin Name	Type	Level	Description	Comment
VDD_3V3	P,I	3.3V +/-5%	Main power supply input	All VDD_3V3 pins must be tied together.
GND	Gnd	0	Ground	All GND pins must be connected to ground.
VDD_BAT	P,I	3.3V +/-5%	"Always-on" supply.	Must be tied to VDD_3V3 unless an external power switch is available. See section 4.13.
nRST_IN	Ctrl,PU	3V3_LVTTL	Reset input, active negative. Module is in reset when low. Short low pulses of less than 1 µs are ignored.	Internally debounced, can be directly connected to a push-button.
MODULE_RDY	O	3V3_LVTTL	Level is high when module is operating, and low when in standby or reset.	Level becomes high about 300 milliseconds after powering / unresetting the module.
1V8_OUT	P,O	1.8V	1.8V output, see below	
SYNC	I	1V8_LVTTL	Reserved. Must always be connected to 1V8_OUT.	

Note that the 2V8_OUT and 2V8_IN pins are exclusively reserved to power the internal TCXO. See section 4.7.

The 1V8_OUT pin is a DC output (120mA max current) which can, for example, be used to power level-shifters for the 1V8_LVTTL signals (EVENT and PPS), see for example section 4.8.

The module can also control an external power switch, to enable standby mode. See section 4.13 for details.

See also the power state diagram in section 5.4.

4.2 Antenna(s)

4.2.1 Main Antenna

The main antenna (which is the only antenna on single-antenna modules) is directly connected to the ANT_1 pad. The ANT_1 input is ESD-protected in the module and carries a DC-voltage to power the antenna, avoiding the need for an external bias-tee. This DC-voltage is imposed to the module via the VANT pad.

In case of an overcurrent condition (e.g. short circuit in antenna cable), the module will first limit the current to about 150 mA and then switch off the antenna supply in about 10 ms. It will periodically retry to switch on the antenna supply until the overcurrent condition has disappeared.

Pin Name	Type	Level	Description	Comment
ANT_1	RF		RF input for main antenna	
VANT	P,I	3–5.5V	DC supply to the ANT_1 antenna. Max current 150mA. DC supply is turned off if overcurrent is detected. If those pads are not connected or if they are tied to GND, there is no DC voltage at the ANT_1 pad.	The two VANT pads should be tied together.

4.2.1.1 ANT_1 Electrical Specifications

DC bias	DC level provided with the VANT pad
Equivalent DC series impedance at the ANT_1 pin	2.5 Ohms typical, 3.0 Ohms max
Antenna current limit	150 mA
ANT_1 pre-amplification gain range[1]	Single-antenna modules: 15-50 dB (AGC gain: 15-50dB) Dual-antenna modules: 15-35dB (AGC gain: 30-50dB)
ANT_1 receiver noise figure[2] (NFrx, see Appendix B)	8.5 dB with 15 dB net pre-amplification 18 dB with 25 dB net pre-amplification 26 dB with 35 dB net pre-amplification 35 dB with 45 dB net pre-amplification
RF nominal input impedance	50 Ohms
VSWR	< 2:1 in all the supported frequency bands

⚠ Never inject an external DC voltage into the ANT_1 pad as it may damage the module. For instance, when using a splitter to distribute the antenna signal to several GNSS receivers, make sure that no more than one output of the splitter passes DC. Use DC-blocks otherwise.

4.2.2 Auxiliary Antenna

In dual-antenna modules, the auxiliary antenna is connected to the ANT_2 pad. In single-antenna modules, ANT_2 is not used and must be tied to ground.

Pin Name	Type	Level	Description	Comment
ANT_2	RF		RF input for auxiliary antenna	To be tied to ground in single-antenna modules

Contrary to the ANT_1 pad, ANT_2 is not ESD-protected and it carries no DC voltage. ESD protection and biasing must be performed externally. See section 4.2.3.2.

4.2.2.1 ANT_2 Electrical Specifications

DC bias	None, ANT_2 is AC-coupled
ANT_2 pre-amplification gain range[1]	15-35 dB (i.e. AGC gain: 30-50dB)
ANT_2 receiver noise figure (NFrx, see Appendix B)	6 dB with 15 dB net pre-amplification 14.5 dB with 25 dB net pre-amplification 21 dB with 35 dB net pre-amplification
RF nominal input impedance	50 Ohms
VSWR	< 2:1 in all the supported frequency bands

[1] The pre-amplification gain is the total gain of the distribution network in front of the module. Typically, this equals antenna active LNA gain minus coax losses in the applicable GNSS bands. The pre-amplification gain can be computed from the AGC gain reported by the module in the `ReceiverStatus` SBF block and shown in the web interface or the RxControl GUI. The conversion formula from the reported AGC gain to the pre-amplification gain is:

Pre-amp gain[dB] = 65 - AGCgain[dB]

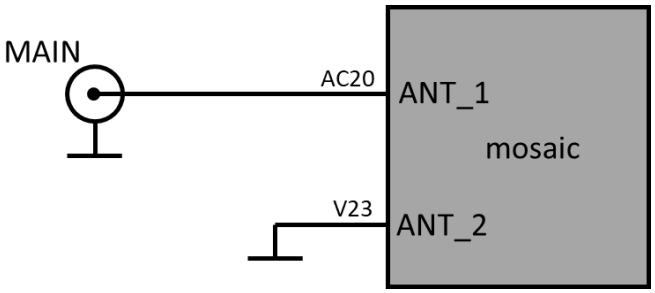
So, if the receiver reports an AGC gain of 30dB, the pre-amplification gain is 35dB.

[2] The listed noise figure is at room temperature. Add 2 dB for the noise figure at the worst temperature corner (85°C)

4.2.3 Typical Application

4.2.3.1 Single Antenna Modules

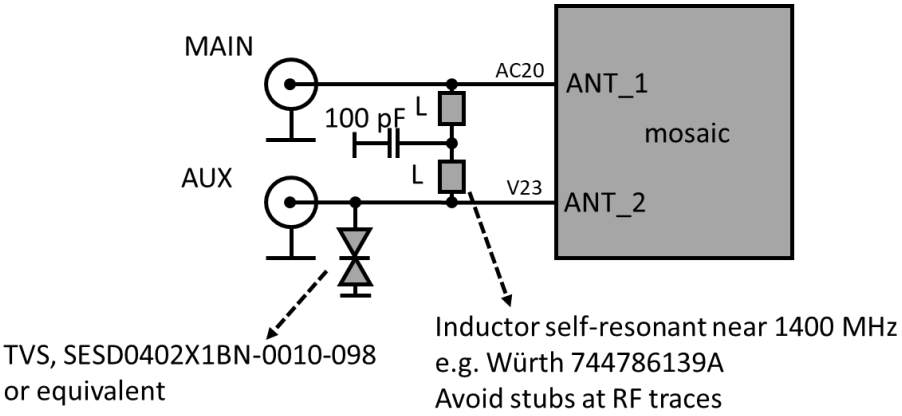
The ANT_1 input is DC-biased and ESD-protected, so that no external component is needed. Make sure to connect the ANT_2 pad to ground.



Refer to 5.5.3 for RF-routing recommendations.

4.2.3.2 Dual-Antenna Modules

The main antenna connects to ANT_1 and the auxiliary antenna to ANT_2. ANT_1 is DC-biased and ESD-protected, while ANT_2 is AC-coupled and unprotected. A recommended application circuit is shown below. With this circuit, the DC bias from the ANT_1 pad is shared between the two antennas. Note that the combined current drawn by both antennas must not exceed 150mA in that case.



Refer to 5.5.3 for RF-routing recommendations.

If the pre-amplification gain is higher than 35dB, it is recommended to put attenuators in the RF path. See Appendix C for instructions.

In addition, the ANT_1 and ANT_2 pre-amplification must not differ by more than 5dB. It is recommended to use the same antenna type for the main and auxiliary antennas, and, as much as possible, to use antenna cables of the same type and length. In case this is not possible, the strongest signal needs to be attenuated, as also described in Appendix C.

4.3 COM Ports

The module provides four serial COM ports. Three of them (COM1 to COM3) support RTS/CTS hardware flow control:

Pin Name	Type	Level	Description	Comment
TXD1	O	3V3_LVTTL	Serial COM1 transmit line (inactive state is high)	
RXD1	I, PU	3V3_LVTTL	Serial COM1 receive line (inactive state is high)	
RTS1	O	3V3_LVTTL	Serial COM1 RTS line.	The module drives this pin low when ready to receive data
CTS1	I, PU	3V3_LVTTL	Serial COM 1 CTS line.	Must be driven low when ready to receive data from the module.
TXD2	O	3V3_LVTTL	Serial COM2 transmit line (inactive state is high)	
RXD2	I, PU	3V3_LVTTL	Serial COM2 receive line (inactive state is high)	
RTS2	O	3V3_LVTTL	Serial COM2 RTS line.	The module drives this pin low when ready to receive data
CTS2	I, PU	3V3_LVTTL	Serial COM3 CTS line.	Must be driven low when ready to receive data from the module.
TXD3	O	3V3_LVTTL	Serial COM3 transmit line (inactive state is high)	
RXD3	I, PU	3V3_LVTTL	Serial COM3 receive line (inactive state is high)	
RTS3	O	3V3_LVTTL	Serial COM3 RTS line.	The module drives this pin low when ready to receive data
CTS3	I, PU	3V3_LVTTL	Serial COM3 CTS line.	Must be driven low when ready to receive data from the module.
TXD4	O	3V3_LVTTL	Serial COM4 transmit line (inactive state is high)	
RXD4	I, PU	3V3_LVTTL	Serial COM4 receive line (inactive state is high)	

Unused COM-port signals can be left floating. Flow control is disabled by default.

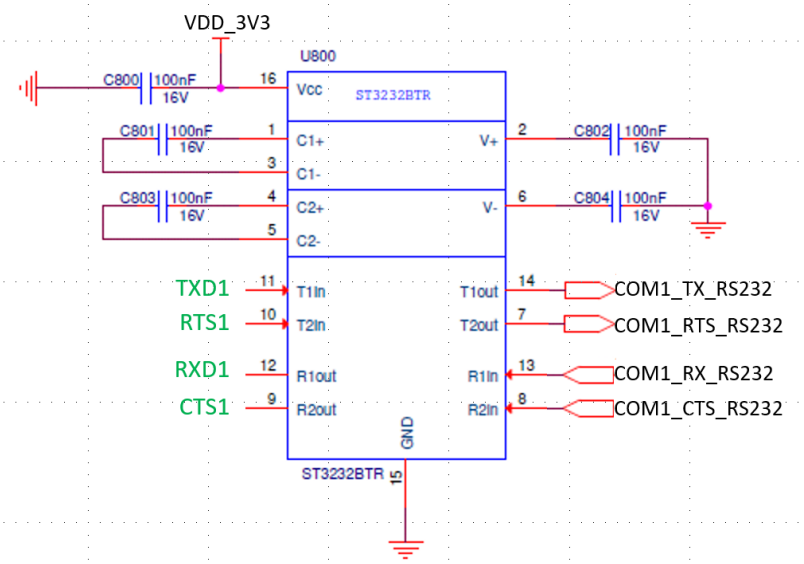
The COM port settings (baud rate, flow control, etc) are set with the **setCOMSettings** user command. The maximum baud rate is 4Mbits/s.

The LVTTL RXD and CTS inputs of the module shall not be driven while its VDD_3V3 input supply is not present.

4.3.1 Typical Application

An example of a circuit to convert the COM1 signals to RS232 level is shown below. In green, the signals to be connected to the mosaic pins. The RTS1 and CTS1 signals can be left unconnected if hardware flow control is not required.

It is recommended to use the same 3V3 source to supply the RS232 transceiver and the VDD_3V3 pins of the module, to ensure that the transceiver outputs are not driven when the module is not powered.



4.4 USB Device Interface

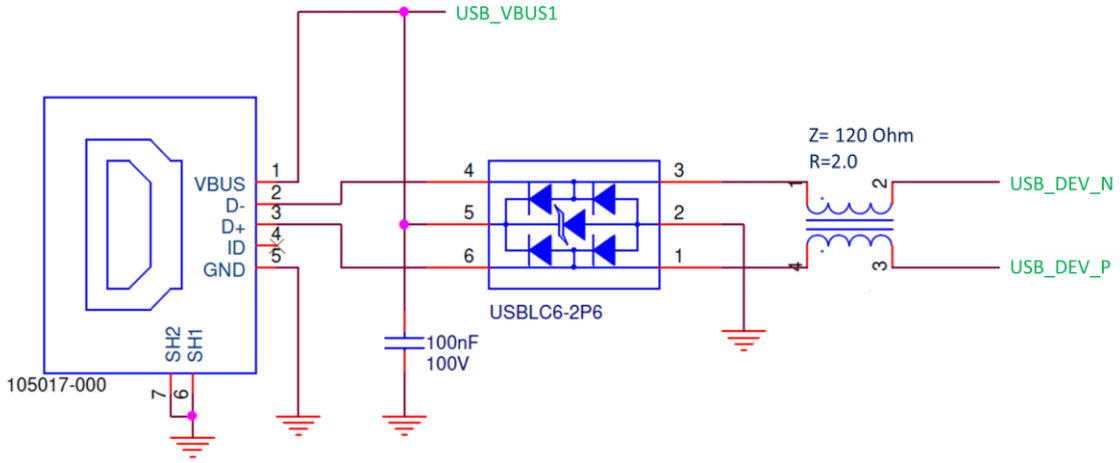
The following pins are used for accessing the module over USB in USB-device mode.

Pin Name	Type	Level	Description	Comment
USB_VBUS1	P,I	4.40V to 5.5V	USB VBUS input. ⚠ This pin cannot be used to power the module. Maximal current drawn by the module is 50 mA. Note: if USB is unused, this pin shall be left floating	This pin powers the integrated PHY of the USB interface.
USB_DEV_N	I/O	USB	USB data signal, negative	
USB_DEV_P	I/O	USB	USB data signal, positive	

USB is configured in USB 2.0 mode (high speed, 480Mbps max).

4.4.1 Typical Application

An example of an USB application circuit with ESD protection is shown below. The user shall make sure to use an ESD-protection and common mode choke compatible with high-speed USB if this is desired, for instance the USBLC6-2 from ST and DLP31SN121ML2L from Murata.



4.5 Ethernet

The module supports full duplex 10/100 Base-T Ethernet communication. The Ethernet PHY and magnetics are to be implemented on the host board. Connection with the PHY is through the RMII interface available on the following pins:

Pin Name	Type	Level	Description	Comment
RMII_CLK	O	3V3_LVTTL	LAN PHY Clock	
MDIO	I/O	3V3_LVTTL	LAN PHY control data	
MDC	O	3V3_LVTTL	LAN PHY control clock	
RMII_RXD1	I, PU	3V3_LVTTL	LAN PHY receive data 1	
RMII_RXD0	I, PU	3V3_LVTTL	LAN PHY receive data 0	
RMII_CRSDV	I, PU	3V3_LVTTL	LAN PHY CRS	
RMII_RXER	I, PU	3V3_LVTTL	LAN PHY RX error	
RMII_TXEN	O	3V3_LVTTL	LAN PHY transmit enable	
RMII_TXD0	O	3V3_LVTTL	LAN PHY transmit data 0	
RMII_TXD1	O	3V3_LVTTL	LAN PHY transmit data 1	
nRST_LAN	O	3V3_LVTTL	LAN reset (low to reset the PHY)	When connecting this pin to enable an Ethernet PHY, add a 10k pull-down.

If Ethernet is not used, all these pins should be left unconnected.

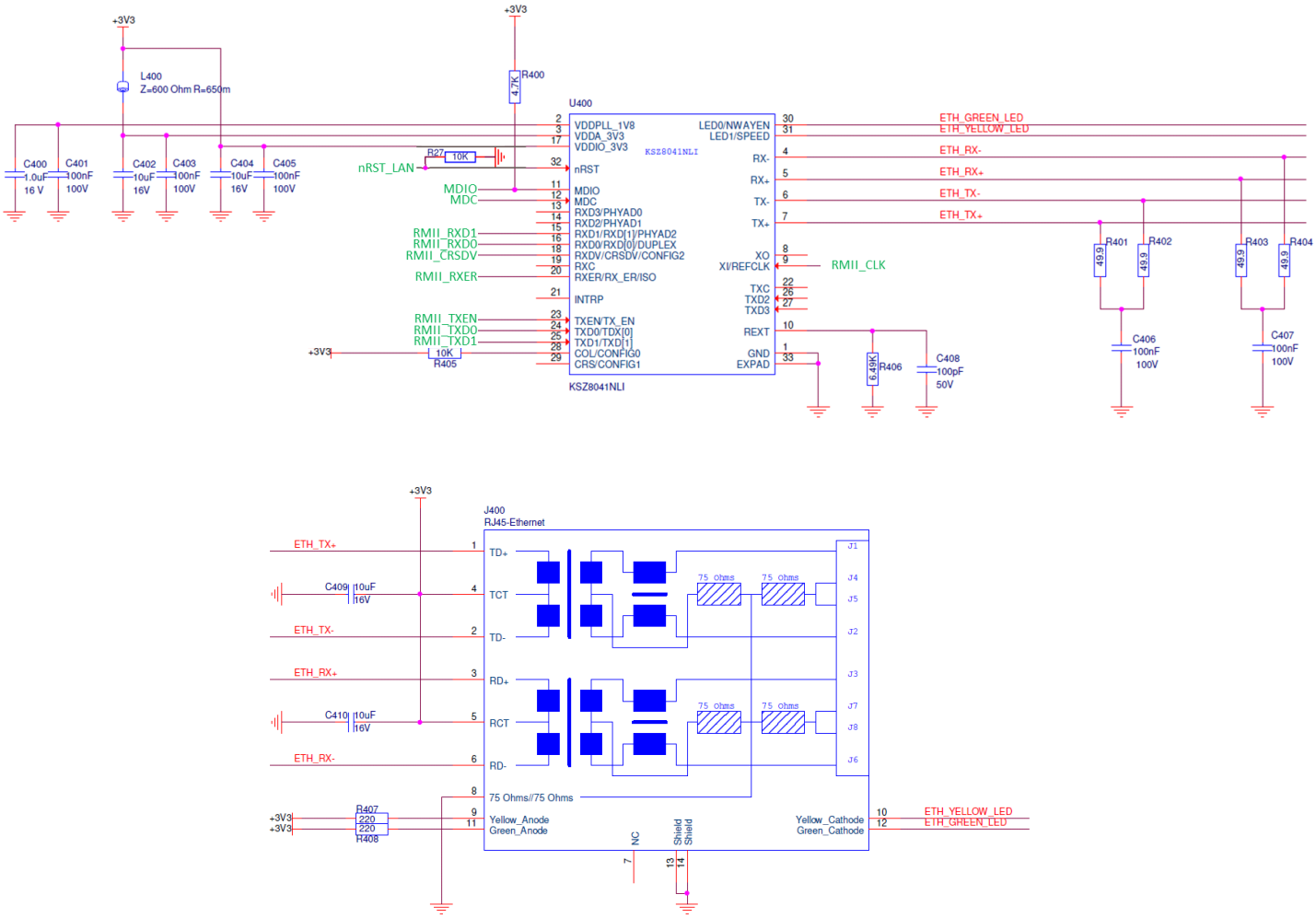
Hostname: the module hostname is based on the last seven digits of the serial number. For example, the hostname of the module shown below is **mosaic-X5-3054938**.

4.5.1 Typical Application

An application circuit using the KSZ8041NLI PHY and a Würth 74990111217 RJ45 connector with integrated magnetics is given below. In green, the signals to be connected to the mosaic pins.

It is recommended to use the same 3V3 source to supply the PHY and the VDD_3V3 pins of the module, to ensure that the PHY output pins are not driven when the module is not powered.

The module also supports other PHYs. An up-to-date list of supported PHY's can be found in Septentrio's Knowledge Base pages:
https://customersupport.septentrio.com/s/article/which-ethernet-phy-does-mosaic-support



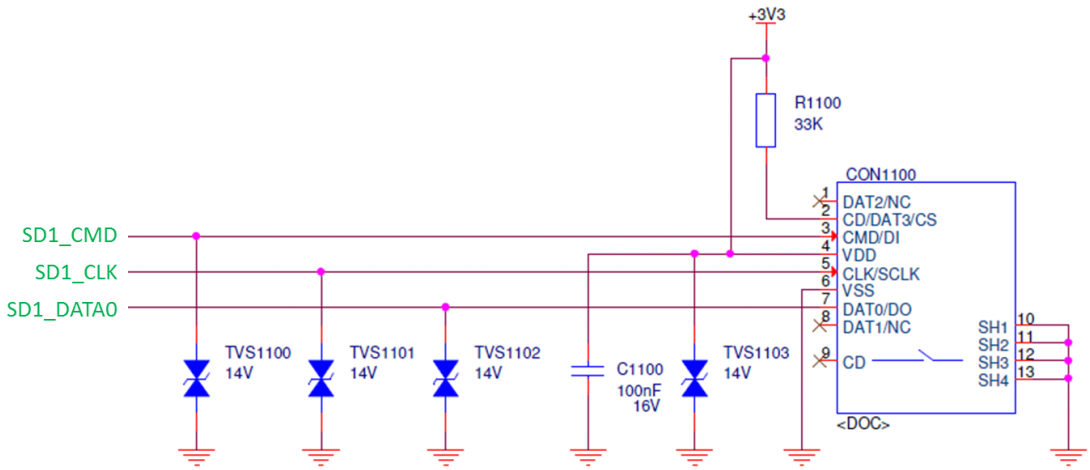
4.6 SD Memory Card

The module can interface to an external SD memory card through the pins listed in the table below.

Pin Name	Type	Level	Description	Comment
SD_CLK	O	3V3_LVTTL	SD card CLK line	
SD_CMD	O	3V3_LVTTL	SD card CMD line	
SD_DAT0	I/O	3V3_LVTTL	SD card DAT0 line	
LOGBUTTON	I, PU	3V3_LVTTL	Toggle logging on/off or mount/unmount the disk. See below	

4.6.1 Typical Application

The module supports the 1-bit SD transfer mode with 3V3 signaling. An example circuit to a 9-pin SD memory card socket is shown below. The maximum clock frequency (SD_CLK) is 33.000 MHz.



4.6.2 Data Logging

Driving the LOGBUTTON pin low for 100 ms to 5 seconds toggles logging on and off.

Driving the LOGBUTTON pin low for more than 5 seconds and then releasing it unmounts the SD card if it was mounted, or mounts it if it was unmounted. The SD card mount status can be checked with the LOGLED pin (see Appendix A).

As the name suggests, the LOGBUTTON is typically interfaced to a mechanical button (though this could also be e.g. an open-collector output or a push-pull output). The module debounces the signal in software, so no external debouncing circuit is required.

See instructions in the Reference Guide for details on how to configure SD card logging. The module is compatible with SD cards of up to 32GB. The file system is FAT32.

When powering off the module while logging, the last seconds of data may be lost. To avoid data losses, it is advised to first unmount the SD card. This can be done in several ways:

1. By entering the command "**exeManageDisk, DSK1, Unmount**" before turning off the module (see the Reference Guide for a description of all the user commands).

2. By driving the LOGBUTTON pin low for at least 5 seconds before turning off the module.

3. By driving the ONOFF pin low for at least 50ms. This puts the module in standby, from where it can be safely switched off. See sections 4.13 and 5.4 for details.

4.7 Clock Frequency Reference

The module can use its internal TCXO frequency reference, or can accept an external frequency reference, bypassing the internal TCXO.

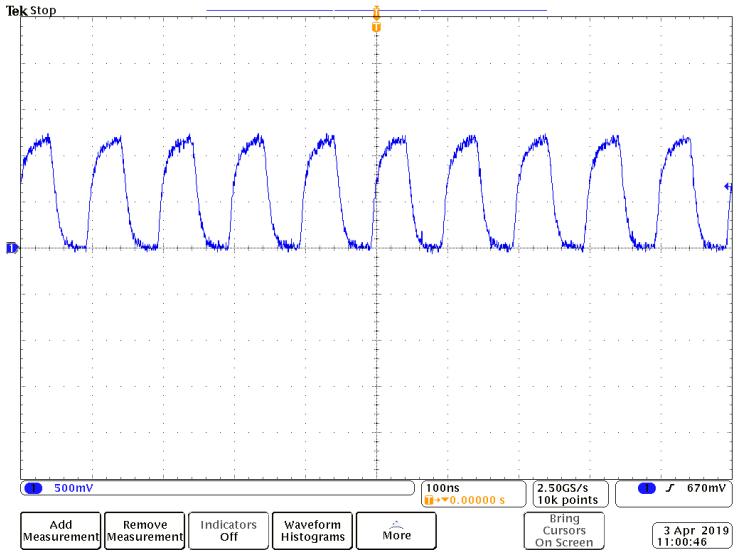
Pin Name	Type	Level	Description	Comment
REF_I	Clk	0.5-1.7Vp-p	Main frequency reference input, DC-decoupled, input capacitance is 8 pF	See section 4.7.2.
REF_O	Clk	1.2Vp-p	Frequency reference output from the internal TCXO	See section 4.7.1.
2V8_OUT	P,O	2.8V	2.8V supply output for the internal TCXO.	Do not power any external device from this pin. It is only intended to connect to 2V8_IN.
2V8_IN	P,I	2.8V	2.8V supply input for the internal TCXO. Typically connected to 2V8_OUT.	
VTUNE	I		Reserved	Leave unconnected.

4.7.1 Using the Internal TCXO

To have the module run on its own TCXO:

- REF_I must be connected to REF_O (those pins are next to each other);
- 2V8_IN must be connected to 2V8_OUT (those pins are next to each other). Do not use the 2V8_OUT for another purpose and do not apply another 2.8V supply to 2V8_IN than the one from 2V8_OUT.

The 10-MHz signal from the internal TCXO is available at the REF_O pin, with peak-to-peak amplitude of 1.2V. The waveform is illustrated in the oscilloscope screen capture below.



4.7.2 Using an External Frequency Reference

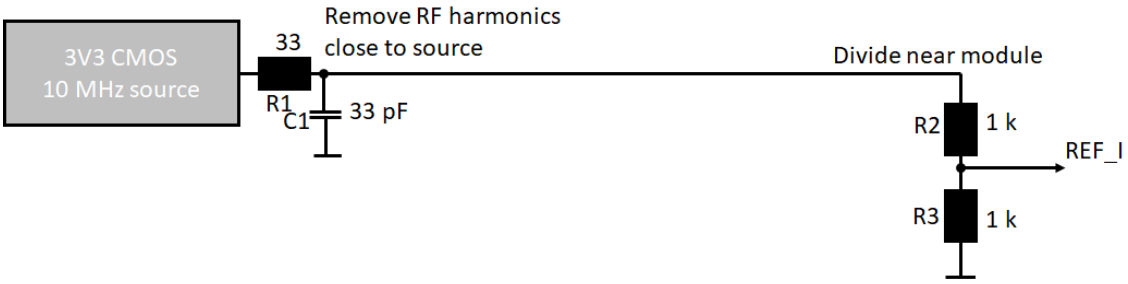
⚠ This feature is only applicable to modules where the Frequency Sync permission is enabled.

To use an external frequency reference:

- 2V8_IN must be left unconnected or tied to ground.
- REF_O and 2V8_OUT are not used and should be left unconnected.

- The 10-MHz frequency reference must meet the following requirements:
  - Frequency tolerance: +/-2.5ppm
  - Allan variance: better than 1ppb (for tau=1s)
  - Phase noise: better than -90dBc/Hz at an offset of 10Hz

- The 10-MHz reference must be fed into the REF_I pin. It is preferably a sine wave or a band-limited square wave. If CMOS or LVTTL signals are used with long traces to the REF_I pin, it is recommended to filter them at the source with an RC filter with a pole near 100 MHz. The level at the REF_I input has to be between 0.5 and 1.7 Vp-p. If a higher signalling voltage is divided with a resistive divider, the impedance level shall be sufficiently low to avoid excessive level drop because of the filtering of the divider with the input capacitance of the REF_I input (8 pF). Below an example circuit. The module has a build-in DC-decoupling capacitor.



When using an external frequency reference, the internal TCXO is turned off and all time bases in the module are driven by the external reference. In particular, the clock drift reported in the `PVTCartesian` or the `PVTGeodetic` SBF block refers to the external clock. It corresponds to the frequency offset of the external reference compared to GNSS time.

Appendix D describes a possible architecture of a disciplined clock based on the mosaic module and Appendix E provides an example of an external reference detection circuit.

4.8 Event Inputs

The module features two event inputs, which can be used to time tag external events with a time resolution of 20ns.

Pin Name	Type	Level	Description	Comment
EVENTA	I, PD	1V8_LVTTL	Event A or TimeSync input. The pull-down is about 200 kOhm.	Leave unconnected if not used
EVENTB	I, PD	1V8_LVTTL	Event B or TimeSync input. The pull-down is about 200 kOhm.	Leave unconnected if not used

Use the **setEventParameters** user command to configure the EVENTx pins (e.g. to set the polarity). For correct detection, the minimum time between two events on the same EVENTx pin must be at least 5ms. The time tag of the pulses seen on the EVENTx pins is available in the `ExtEvent` SBF block.

Note the timing signals use 1.8V logic. If 3.3V logic would be required, the EVENT-signals can be generated via a resistive divider, considering the integrated pull-down (see 3.4.2).

They could as well be created via a level shifter, using the 1V8_OUT output from the module to supply the module side.

4.9 TimeSync

If the Time Sync permission is enabled, the EVENTA or EVENTB input (see section 4.8) can be configured as TimeSync source using the **setTimeSyncSource** command. When an event pin is configured as TimeSync source, the module expects to see a one-pulse-per-second (1PPS) signal on that pin. The module initializes its internal time scale with the first PPS pulse it sees, with a possible offset of an integer number "*k*" of milliseconds. That offset of *k**1ms is introduced to maintain the receiver time base close to GNSS time, regardless of the timing of the external PPS pulse. *k* is the time difference between the external PPS and the nearest GNSS second boundary, rounded to the millisecond. If the external PPS is well aligned with GNSS time (deviation smaller than 0.5 ms), *k* is zero. *k* can be measured by connecting the external PPS to both EVENT pins, one of them configured in TimeSync mode, and the other in time tagging mode, as explained in section 4.8.

TimeSync is typically used in conjunction with ExtFreq (see section 4.7.2), to align the frequency and time (modulo 1ms) of the module with that of an external clock.

In addition to the *k**1ms offset, there is a delay of 15 to 50 ns between the PPS pulse at the EVENT pin and the module internal time base. That delay is dependent on the phase difference between the 10 MHz frequency at the REF_I pin and the PPS pulse at the EVENT pin. It is possible to measure this delay by synchronizing the PPS OUT pulse with the internal time base, with the **setPPSParameters,,,,RxClock** command.

4.10 PPS output

Pin Name	Type	Level	Description	Comment
PPSO	O	1V8_LVTTL	PPS output. Max output current: 10 mA. Polarity and rate user selectable. During start up, this pin is in high-Z mode. See Reference Guide for operating instructions. Default pulse duration: 5ms.	

The polarity, frequency and pulse width can be set with the **setPPSParameters** command.

The PPSO signal uses 1.8V logic. It can be level-shifted if 3.3V logic is required (e.g. with SN74AVC4T245RSV).

The PPSO signal is briefly driven high during startup of the module (for about 1 ms), then gets high-impedant while the module is starting up. It finally gets driven to the intended level (low or high depending on the user-selected PPS polarity) after a few seconds. If this start-up behavior is undesirable, it can be shielded by a buffer (or level shifter) with an output enable. The output enable can be controlled with the MODULE_RDY pin of the module. The MODULE_RDY signal gets high about 300ms after applying power to

VDD_3V3. The input and output of the buffer should be pulled-up or pulled-down depending on the desired inactive state of the PPSO signal.

4.11 General Purpose Output (GPx)

The GP1 and GP2 pins are general purpose digital outputs, of which the level can be programmed with the **setGPIOFunctionality** command.

Pin Name	Type	Level	Description	Comment
GP1	O	3V3_LVTTL	General purpose output. GP1 in **setGPIOFunctionality** command.	
GP2	O	3V3_LVTTL	General purpose output. GP2 in **setGPIOFunctionality** command.	

During the first seconds after powering up the module, these pins are in tristate. Use an external pull-down or pull-up resistor to have the desired level during boot.

The GPx pins can drive a maximum current of 10mA.

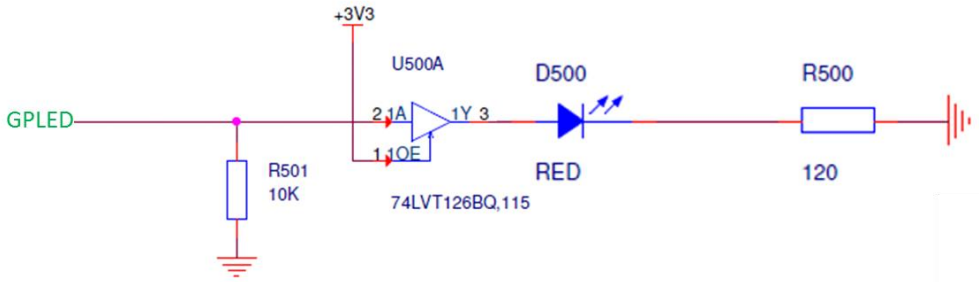
4.12 LEDs

The LED pins can be used to monitor the module status. They can be used to drive external LEDs. It is assumed that the LED lights up when the electrical level of the corresponding pin is high. See also Appendix A.

Pin Name	Type	Level	Description	Comment
GPLED	O	3V3_LVTTL	First general purpose LED. Max output current: 10 mA; output impedance: 20 Ohms	
GPLED2	O	3V3_LVTTL	Second general purpose LED. Max output current: 10 mA; output impedance: 20 Ohms	
LOGLED	O	3V3_LVTTL	Internal logging status indicator. Max output current: 10 mA; output impedance: 20 Ohms	

During boot, i.e. during the first seconds after powering the module, the state of the LEDs is not defined. Use a pull-down or pull-up resistor to force a desired state.

An example of a circuit with a 10k pull-down and a driver is shown below.



4.13 Standby

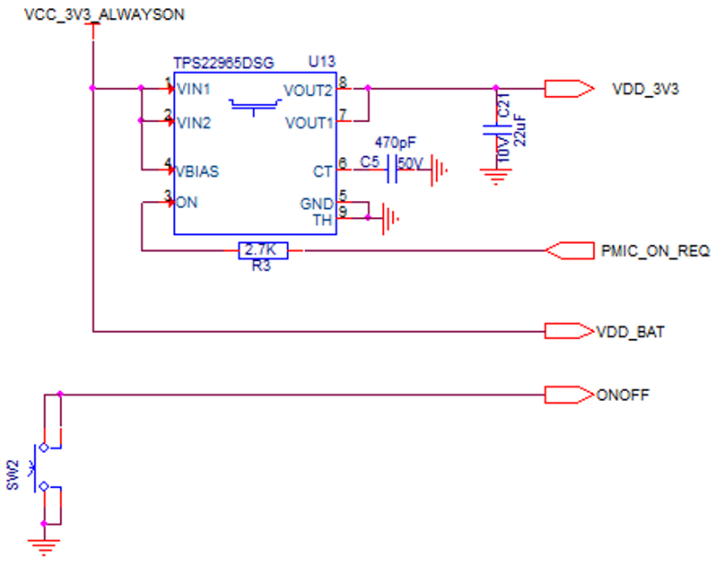
It is of course possible to power off the module by switching off the VDD_3V3 and VDD_BAT supplies. However, this abrupt power interruption could cause data losses when logging on an external SD card.

The module also supports standby mode, where it controls an external power switch and turns itself off in a controlled way. This functionality involves the following pins:

Pin Name	Type	Level	Description	Comment
VDD_3V3	P,I	3.3V +/-5%	Main power supply input, controlled by the external power switch	All VDD_3V3 pins must be tied together.
VDD_BAT	P,I	3.3V +/-5%	Always-on power supply, which must remain available when VDD_3V3 is turned off by the external power switch	
ONOFF	I, PU	3V3_LVTTL	Typically connected to a push-button to toggle between active and standby mode. Toggling occurs when the ONOFF pin is driven low for at least 50ms.	Internally debounced
PMIC_ON_REQ	O	3V3_LVTTL	Typically connected to the control pin of an external power switch. The power switch is expected to enable VDD_3V3 when PMIC_ON_REQ is high, and to disable VDD_3V3 when it is low.	
MODULE_RDY	O	3V3_LVTTL	Level is high when module is operating, and low when in standby or reset.	Level becomes high about 300 milliseconds after powering up, unresetting, or waking up after standby

The external power switch is optional. When not using an external power switch, always connect VDD_BAT together with VDD_3V3.

An example optional circuit with an external power switch and an on/off push-button is shown below.



The module can be put in standby by either:

- Entering the **exePowerMode, standby** user command;
- Driving the ONOFF pin low for at least 50ms (i.e. pressing the button for at least 50ms).

After standby is requested, the module terminates all running processes, unmounts the external SD card (if applicable) to avoid any log file corruption, and drives the PMIC_ON_REQ pin low to turn off the main power supply (VDD_3V3). The module power consumption in standby is <5mW. The current state of the module (standby or active) can be monitored with the MODULE_RDY pin. MODULE_RDY is low during standby.

When in standby, driving the ONOFF pin low for at least 50ms wakes up the module. The module drives the PMIC_ON_REQ high, and restarts in the configuration stored in the boot configuration file.

The ONOFF pin is internally pulled up and has a built-in debouncing circuit.

Do not drive a non-zero voltage into input pins (pins type “I” in the tables in chapter 3) when the module is in standby, i.e. when the VDD_3V3 supply is turned off.

Note that the ONOFF pin can also be used without external power switch (i.e. when VDD_3V3 is tied to VDD_BAT). The module will then stop all software and unmount the external SD card, but will not enter low power consumption. It will automatically wake up again after about 2 minutes.

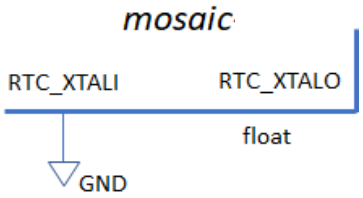
See also section 5.4.

4.14 RTC

The RTC_XTALI and RTC_XTALO pins are reserved to connect an external 32.768 kHz crystal.

Pin Name	Type	Level	Description	Comment
RTC_XTALI	I		Crystal oscillator input terminal	Future functionality, connect to ground in present version of the module
RTC_XTALO	O		Crystal oscillator output terminal	Future functionality, leave unconnected in present version of the module

Note that this functionality is currently not available. RTC_XTALI should be tied to ground, and RTC_XTALO left floating:



5 mosaic Integration

5.1 Minimal Design

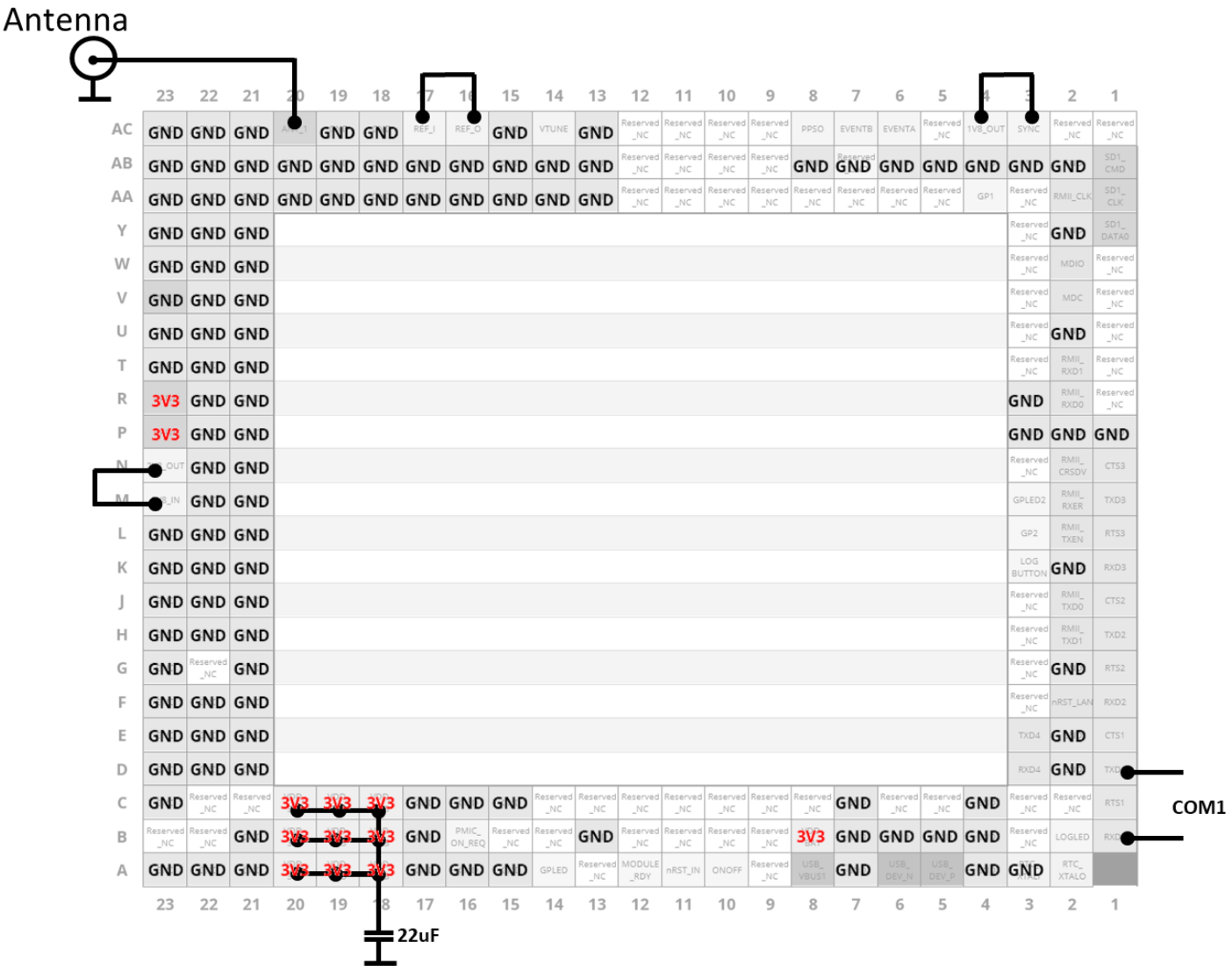
A minimal design for single-antenna and dual-antenna modules is shown below. In both cases:

- All ground pins and the pins marked “Reserved_GND” are connected to ground (GND).
- A 3.3VDC supply is provided to the VDD_3V3 pins and to the VDD_BAT pin. A 22µF decoupling capacitor is recommended.
- To provide power to the antenna(s), the VANT pins are also connected to the 3.3V supply.
- The 2V8_IN and 2V8_OUT pins are connected, as no external frequency reference is used (see section 4.7).
- The REF_I and REF_O pins are connected for the same reason.
- 1V8_OUT is connected to SYNC (this must always be the case).
- Pin A3 (RTC_XTALI) needs to be connected to ground.
- All other pins are left unconnected.

For easier debugging during host design development, it is recommended to always route at least one of the COM ports to test pads or a test header.

5.1.1 Single-Antenna Modules

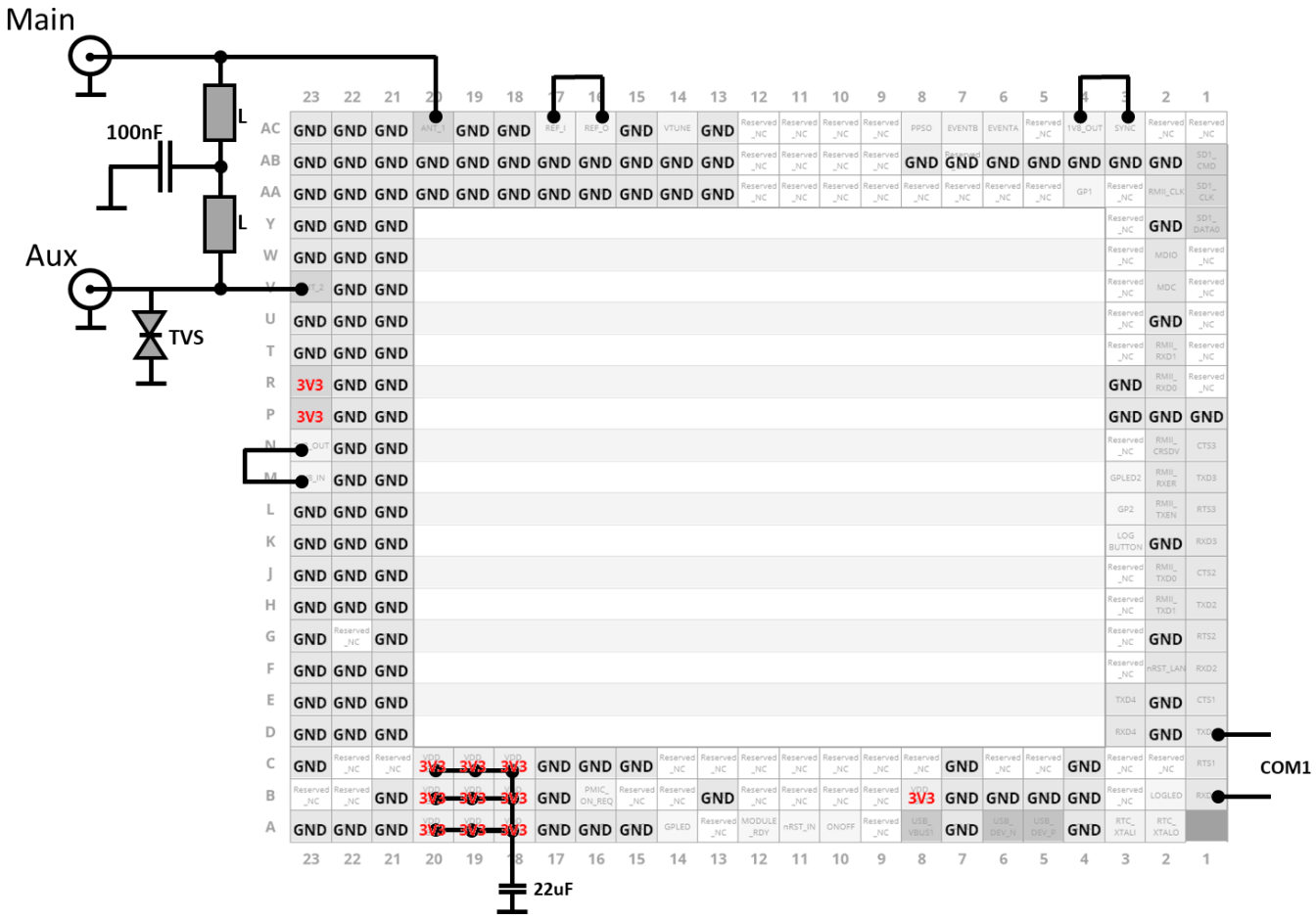
In single antenna mosaic modules, the ANT_2 pin (V23) must be tied to ground.



5.1.2 Dual-Antenna Modules

The main antenna connects to ANT_1 (AC20) and the auxiliary antenna connects to ANT_2 (V23). DC supply is provided through the ANT_1 pin, and the biasing circuit to supply the auxiliary antenna is shown (see also section 4.2.3.2).

L: Inductor self resonant near 1400MHz, e.g. Würth 744786139A.
TVS: Transient voltage suppression diode, SESD0402X1BN-0010-098 or equivalent.



Note that the combined current drawn by both antennas must not exceed 150mA.

5.2 Electrical Recommendations

- All ground pins must be connected.
- Do not drive a non-zero voltage into input pins (pins type “I” in the tables in chapter 4) when the module is not powered or when it is in standby (see section 4.13).
- When pull-up/down resistors are needed, use 10 kΩ.
- Unused pins (e.g. pins of an unused interface) must be left unconnected unless explicitly mentioned otherwise.

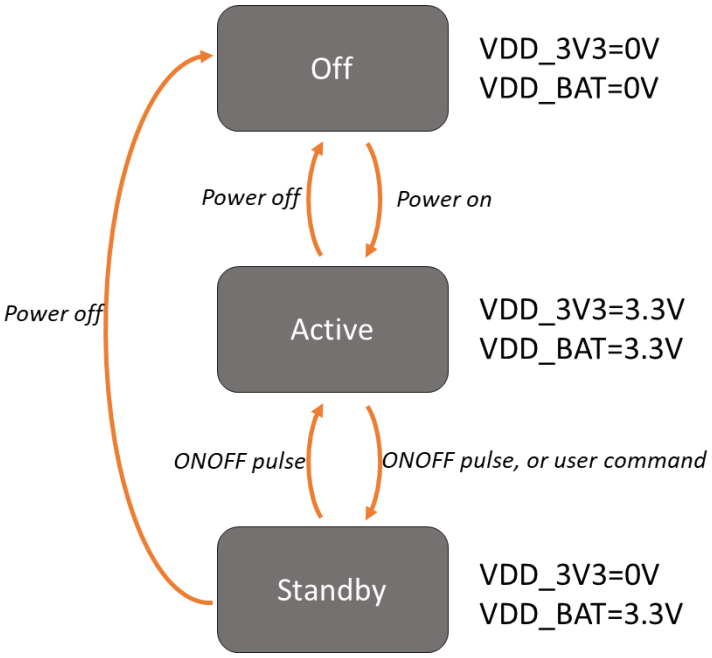
- Many pins are reserved, which means that their functionality is proprietary or is not supported yet by the firmware. Reserved pins are marked “Reserved_NC” and “Reserved_GND”. The Reserved_NC pins must be left unconnected. The Reserved_GND pin (i.e. only AB7) must be tied to ground.

5.3 Decoupling

The VDD_3V3 supply shall be decoupled with at least a 22 µF capacitor with proper voltage rating. The other supply terminals don’t need external decoupling.

5.4 Power States

The module can be in three different states: off, active or standby.



When off, the module is completely turned off. In active state, it is operating with all functions active. Standby state is similar to off, the main difference being in the transition from the active state:

- When going from active to off, recent data logged to an external SD card may be lost (see section 4.6).
- When going from active to standby, all logging tasks are terminated and the SD card is cleanly unmounted.

The standby state is optional and only available if the host design supports it. See section 4.13 for details.

5.5 Layout Recommendations

5.5.1 Coplanarity

It is important to avoid warpage of the motherboard on which the module will be soldered. More in particular:

- Use a symmetrical layer stack
- Make sure layers opposite from the center of the board have a similar amount of copper (copper-balancing).
- Avoid iron-based soldered shielding cans in the proximity of mosaic
- If the motherboard thickness is 1.2 mm or less, it needs to be supported during reflow.

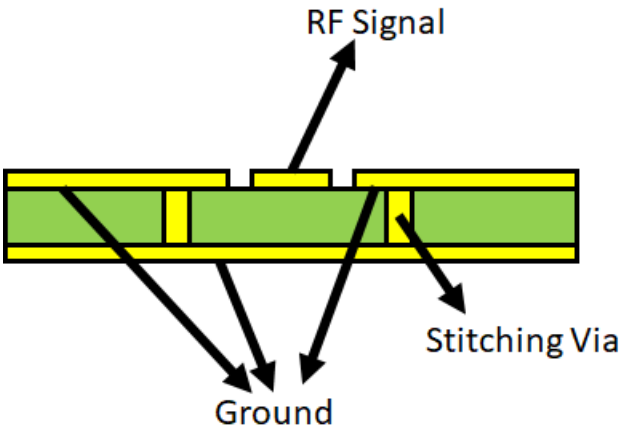
5.5.2 Power

The power trace to the VDD_3V3 terminals should be sufficiently wide to avoid excessive voltage drop. The resistance of the trace to the power supply shall be less than (<minimum supply voltage> - 3.135V)/0.5A.

Use a ground plane.

5.5.3 Antenna Inputs

The antenna input traces shall be routed as a 50-ohm coplanar waveguide with ground, as in the picture below. It is best to use stitching vias every few mm for good ground coherence. The width of the trace to set the impedance to 50 ohm can be calculated with online tools (e.g. https://chemandy.com/calculators/coplanar-waveguide-with-ground-calculator.htm). Usually it is best to use the top-layer for the coplanar waveguide and the second layer for ground.



The antenna trace to ANT_1 can be directly routed to the desired type of coax connector, as all protection circuitry is integrated in mosaic.

For the dual-antenna module, beware that the ANT_2 pin is not protected, and a TVS diode is recommended. See reference design in section 4.2.3.2.

5.5.4 Avoiding Self-Interference

Antenna input connections are sensitive to interference from higher harmonics of other signals on the board. Even clock signals of just a few MHz can produce harmful harmonics at GNSS frequencies (1155-1300 MHz and 1540-1610 MHz).

It is best to keep antenna input traces short, to reduce the area in which signals can be picked up. Stitching vias at the input trace could be arranged as a via fence to shield it from interference.

Furthermore, it is important to avoid digital signals in the MHz-range (SDIO, RMII, MDIO,...) from running close to antenna inputs.

If an external frequency reference is used, it will get close to the antenna input because of the proximity of the REF_I and ANT_1 pad. This is not a problem if it doesn't have many harmonics. It can however cause issues if the reference signal is originating from a high-speed buffer or comparator. This can be avoided at circuit level, by filtering the signal with an RC-filter near the source (see section 4.7.2).

Most self-interference issues relate to radiated interference into a collocated GNSS-antenna. The following applies when the GNSS antenna is closer than 1 meter from electronics which are not in a shielded box:

- The SDIO, RMII and MDIO signals of mosaic can cause harmful radiated interference if not properly routed. In designs with a collocated antenna, these signals shall preferably be routed in an inner layer of the board, shielded by ground planes or a ground copper pour at top and bottom layers, connected with stitching vias. This approach puts them in a Faraday cage. Also avoid passing these signals though an unshielded board-to-board connector if there is no shielding at system level, like a metal housing or shielding can.

- The same holds for other high-speed digital signals in other electronics on the motherboard, like memory busses and clock signals. They should also be routed in an inner layer, flanked with cupper pours connected to ground.

- Large processor and memory chips sometimes already radiate via the bondwires inside their package. Connectors like SD card sockets and radio-module sockets also tend to radiate. It's best to put these components at the side of the board facing away from the collocated antenna. In this way the ground-layer will shield them. Alternatively, they could be placed underneath an EMI shielding can. There is less of a concern if the associated clock frequencies have no harmonics in the GNSS bands.

See also Appendix D.

6 Product Handling

6.1 ESD Precautions

The mosaic module is sensitive to electrostatic discharge (ESD). Although it has a limited protection, it should only be manipulated in an ESD-safe environment and using ESD-safe tools and equipment. These tools are typically marked with the following symbol:

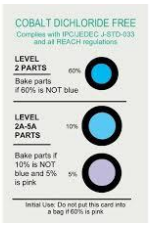
The mosaic module should be stored and handled in the original package (preferably) or in a conductive foam shorting all pads.

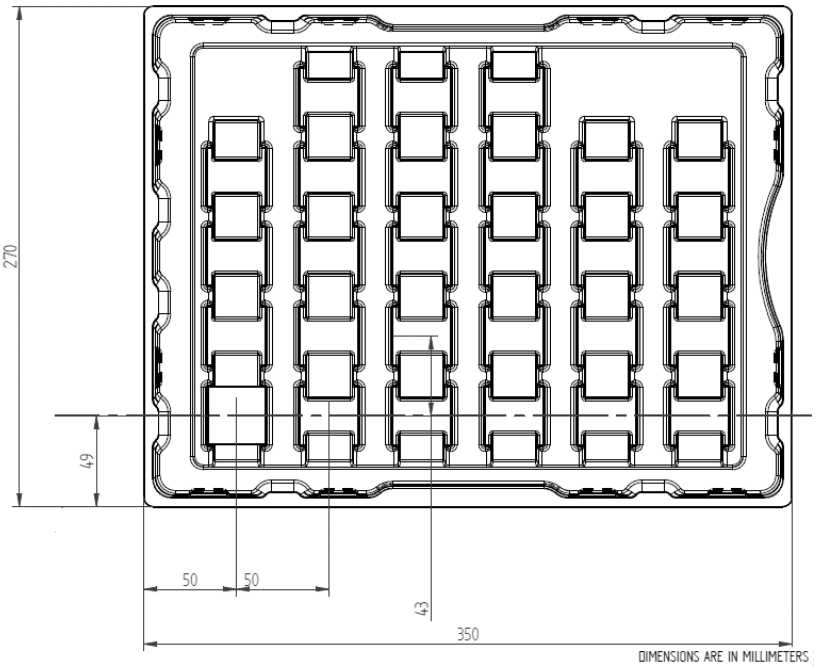
6.2 ROHS/WEEE NOTICE

Septentrio receivers and modules are compliant with the latest WEEE, RoHS and REACH directives. For more info see www.septentrio.com/en/environmental-compliance.

6.3 Packaging

Mosaic modules are delivered on a tray in a dry pack, with 27 modules per tray.





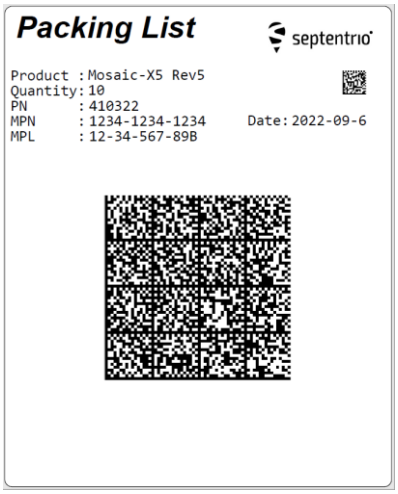
Package contents:

- 27 mosaic modules
- 1 humidity indicator
- 1 desiccator bag
- Packing list Label
- Process lot label
- MSL level label

6.3.1 Packing List Label

The labeling gives product information:

- **Product:** mosaic variant with hardware revision
- **Quantity:** number of modules in the bag
- **PN:** Septentrio Part Number
- **MPN:** Manufacurer Part Number
- **MPL:** Manufacturer Product Lot
- **Date:** Packaging Date



6.3.2 MSL Level Label

The labeling gives information about:

- Moisture Sensitivity Level and Floor Life
- Storage conditions

6.4 Storage

Dry-pack shelf life is according to JEDEC standard J-STD-033 with 12 months at < 40°C and < 90% relative humidity (RH). After the 12-month period, baking is recommended prior to reflow on customer boards.

The moisture sensitivity level (MSL) is 3.

If the dry pack has been opened for more than 168 hours or can no longer be considered dry, the modules must be baked according to JEDEC standard J-STD-033 Table 4-1 Reference Conditions for Drying Mounted or Unmounted SMD Packages. The recommended baking condition is 25 hours at 90°C <= 5% RH.

Oxidation Risk: Baking may cause oxidation and/or intermetallic growth of the terminations, which if excessive can result in solderability problems during board assembly. The cumulative bake time at a temperature greater than 90°C and up to 125°C should not exceed 96 hours.
Bake temperatures higher than 125°C are not allowed.

The 27-position tray cannot sustain baking temperature. The mosaic modules have to be baked separately from the shipment tray.

6.4.1 Note for Small Quantities

For small quantities requested for prototype usage, Septentrio or Septentrio distributors may not be able to supply the modules in dry-pack packaging. In that case, the customer should consider that the components have exceeded their floor life. To prevent damaging the modules during soldering, they need to be baked prior to any reflow.

6.5 Sticker and Identification

The 2D barcode contains the module hardware version and serial number, e.g:

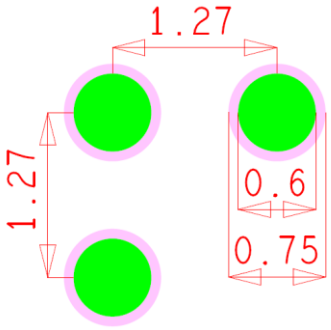
MOSAIC-X5GRB-0051-1000-BA3P2SN19293054938

The serial number is also printed under the barcode.

6.6 Soldering

6.6.1 Solder Mask

Non-solder mask defined (NSMD) pads are recommended, with a clearance of 75µm between the copper pad and the solder mask, as shown in the below figure. The copper pads are in green, the (negative) solder mask is in pink. Dimension in millimeters.



The GND and VDD_3V3 pins are an exception in this respect. They can be solder mask defined, allowing to route them using a plane.

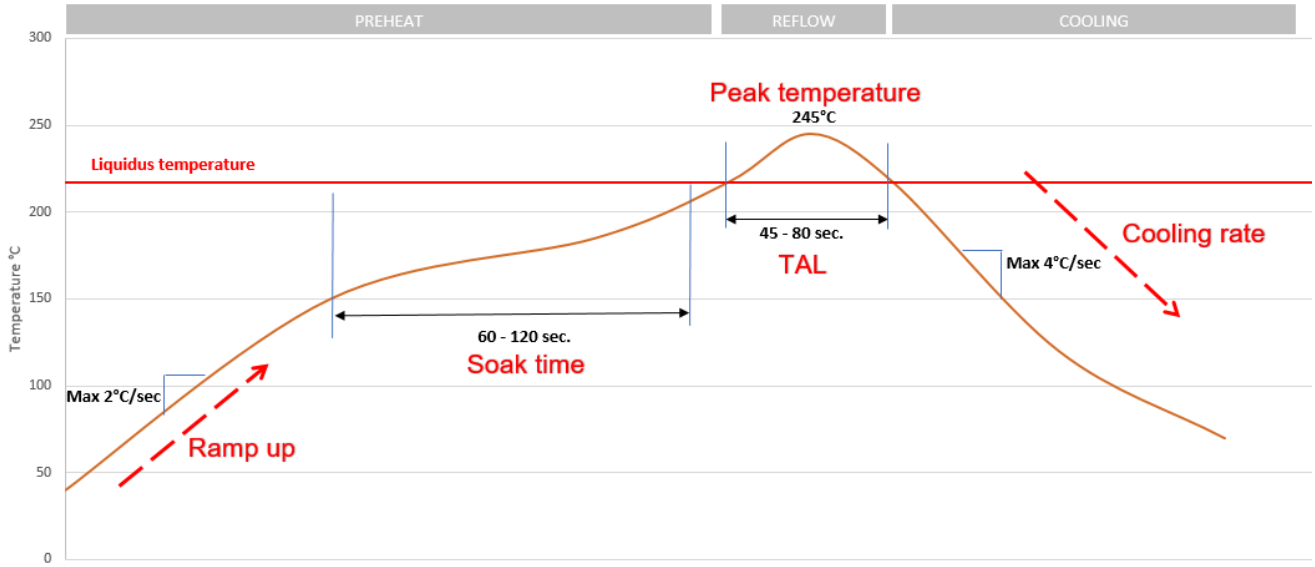
6.6.2 Reflow Profile

Reflow soldering is the soldering method recommended to assemble mosaic modules.

The recommended temperature profile is specified with the graphic below. Refer also to “IPC-7530A: Guidelines for Temperature Profiling for Mass Soldering Processes (Reflow and Wave)”.

The final reflow profile shall be based on leadfree process and depends on parameters such as the soldering paste, host board parameters (shape, thickness, etc...) and oven capabilities.

Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.



Region	Guideline
Ramp up	**max 2 °C/sec**
Soak time	**60-120 sec**
Time Above Liquidus (TAL)	**45-80 sec**
Peak temperature	**245 °C**
Cooling rate	**max 4°C/sec**

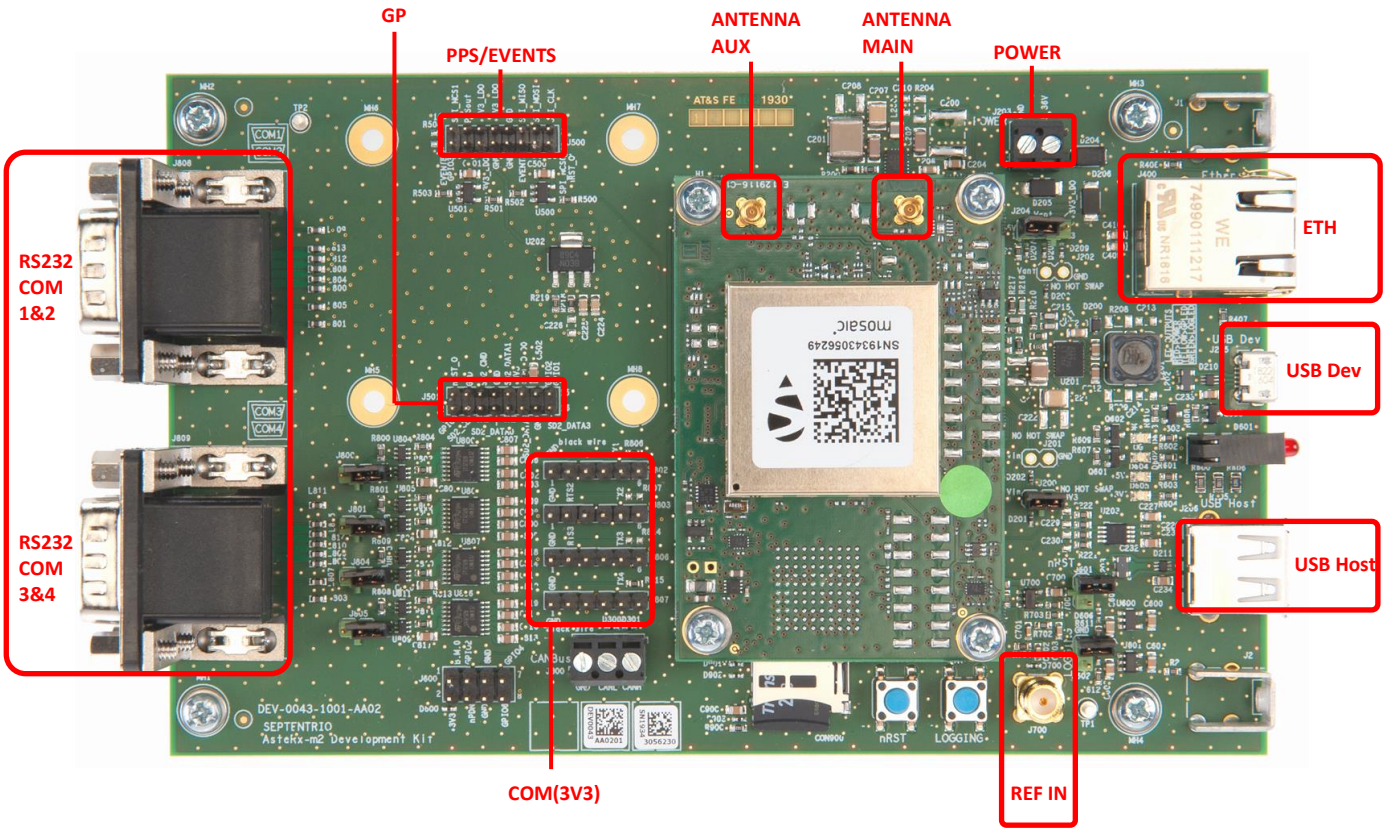
Don't use glue underneath the component, as this might lift the component and jeopardize bonding. Cleaning the module (water, ultrasonic, solvent,...) is not allowed as it could affect its performance.

The recommended stencil thickness is 0.150 mm (6 mils). In any case, it shall not be less than 0.125 mm (5 mils).

Mount the part with the largest available placement nozzle, attached to the center of the shield. Use the slowest possible speed of the pick and place machine.
When implemented on a double-sided PCB, the mosaic module has to be assembled during the final reflow cycle and cannot be reflowed when located on the bottom side of the board.

If the motherboard thickness is 1.2mm or less, it is recommended to support the assembly during the reflow process to minimize bow of the motherboard.

7 Development Kit



The mosaic Development Kit is composed of the mosaic module soldered on an interface PCB (GTB-0051), itself plugged on the DevKit board (DEV-0043).

DevKit Part Number: **410331P3161** (including antenna and accessories).

7.1 Header Types

All headers have a pitch of 2.54mm, with the exception of J500 (PPS/EVENTS) and J501 (GP). Those headers have a 2mm pitch.

7.2 Powering the DevKit

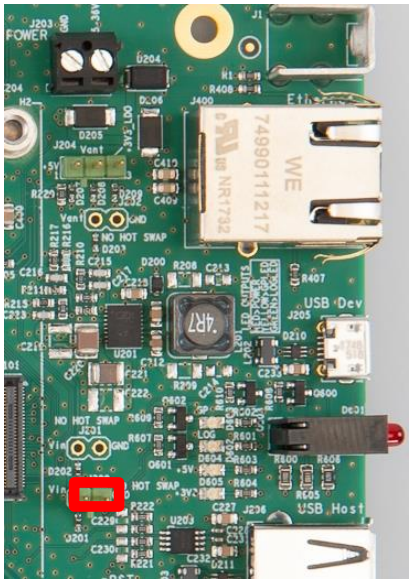
There are two ways to power the DevKit:

1. From the USB Dev connector (J205). This allows powering the board from a PC or from a standard phone-charger adapter. The supported USB voltage range is 4.5V-5.5V.
2. Using the POWER connector (J203). The supported voltage range is 5-36V.

When powering from the USB Dev connector, it is recommended to use the USB cable provided with the DevKit. Low-quality USB cables often suffer from excessive voltage drop, preventing correct operation.

It is safe to provide power to both connectors in parallel. The DevKit will use the source with the highest voltage.

Make sure that a jumper is placed on header J200, as shown below. Otherwise the DevKit will be powered, but not the mosaic module.



To measure the power consumption of the mosaic module (excluding the contribution from the DevKit and the antenna, but including a small contribution from the interface board, remove the jumper on J200 and connect the two pins to the probes of a multimeter in current-sensing mode. Measure the current flowing between the two pins and multiply it by 3.3V to obtain the power consumption. It is recommended to set the multimeter in high ampere setting to keep the voltage drop as low as possible.

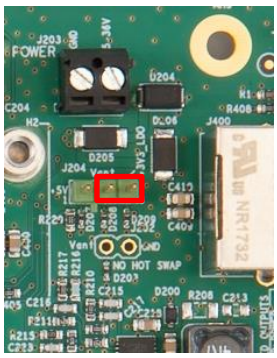
7.3 Antenna Connectors

There is no antenna connector on the DevKit. The antenna(s) must be connected directly to the u.FL or MMCX antenna connector on the mosaic interface board.

The DC voltage (5V or 3.3V) at the antenna connectors is determined by the position of the jumper on header J204, as shown below.

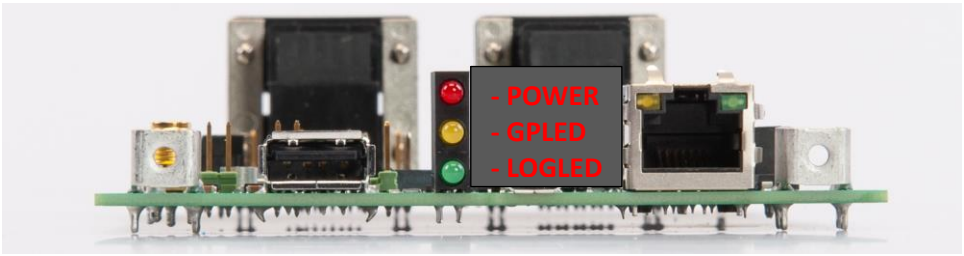
Vant = 5V

Vant = 3.3V



The jumper can be removed if the antenna does not need to be powered by the module. In that case, there is no DC voltage at the antenna connector.

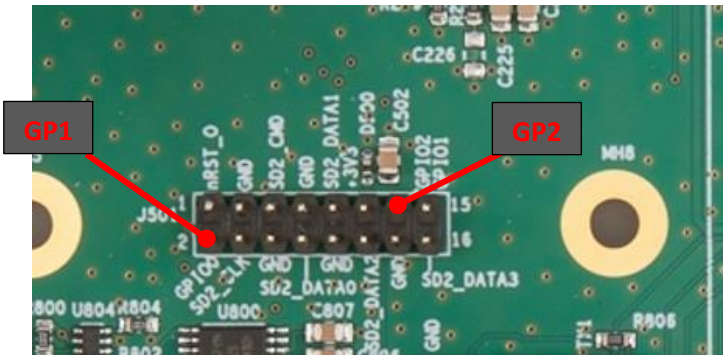
7.4 LEDs and General Purpose Output Pins



The POWER LED lights when the DevKit is powered.

The GPLED and LOGLED are connected to the homonymous pins of the mosaic module. See section 4.12 for the pinout, and Appendix A for a description of the LED behavior. The GPLED2 LED is not available on the DevKit.

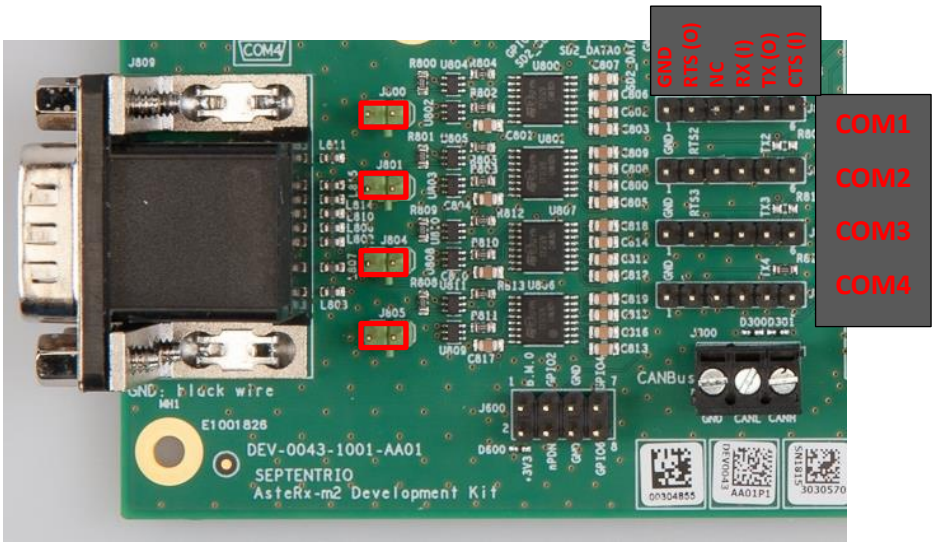
The 3.3V GP1 and GP2 outputs are available on the J501 header (2x8 2mm-pitch DIL).



7.5 COM Ports

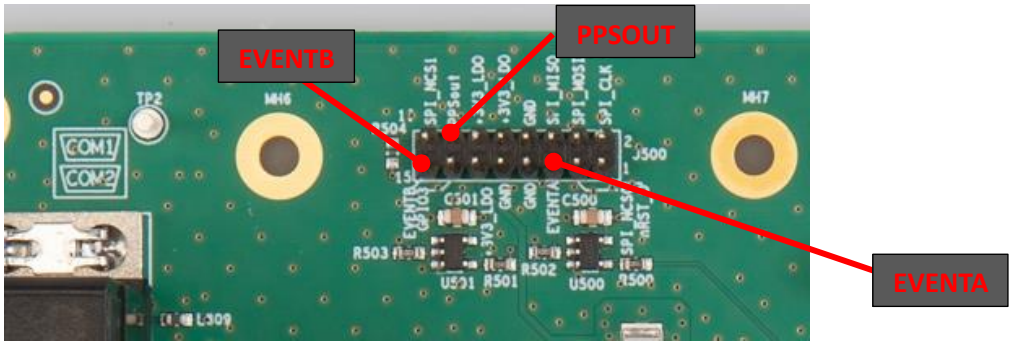
By default, the four COM ports of the mosaic module are routed to the four DB9 connectors of the DevKit. Electrical levels on the BD9 conform to the RS232 standard. RTS/CTS lines are supported only on COM2 and COM3 (the mosaic has RTS/CTS lines on COM1 as well, but they are not routed to the DevKit). Connection to a PC is done through a null-modem cable.

Alternatively, 3.3V TTL signals are available through four 6-pin 2.54mm pitch headers, as shown below. The pinout is compatible with standard FTDI 6-pin SIL connectors. To route a COM port to the 6-pin header instead of the BD9 connector, a jumper must be placed on J800 (COM1), J801 (COM2), J804 (COM3) and/or J805 (COM4). Only those COM ports for which the jumper is placed are routed to the 6-pin header. The other COM ports are still routed to the DB9 connectors, using the RS232 levels.



Note that, when using the DB9 connectors, the baud rate must not be larger than 230400baud. This limitation does not apply to the TTL signals.

7.6 PPS Out and Event Inputs



The PPSout pin of header J500 (2x8 2mm-pitch DIL) is connected to the PPSO pin of the mosaic module through a 1.8V to 3.3V level shifter. The PPS level at the header is 3.3V.

The EVENTA and EVENTB pins of J500 are connected to the EventA and EventB pins of the mosaic through a level shifter to 1.8V. The voltage level at the header pins must be between -0.5V and +6V. These pins are pulled-down by a 100kOhm resistor.

7.7 Ethernet

The DevKit supports 10/100 Base-T Ethernet. It is not possible to power the DevKit through the Ethernet connector.

The development kit is compliant with EU EMC standards (EN303413) provided the Ethernet interface is disabled (with the **setEthernetMode** user command). When the Ethernet interface is enabled, harmonics from the RMII interface slightly violate this regulation, as they radiate via the 60-pins board-to-board connector. It is up to the integrator to take the necessary precautions to avoid EMC violations in this case (e.g. use shielded box).

7.8 USB Dev

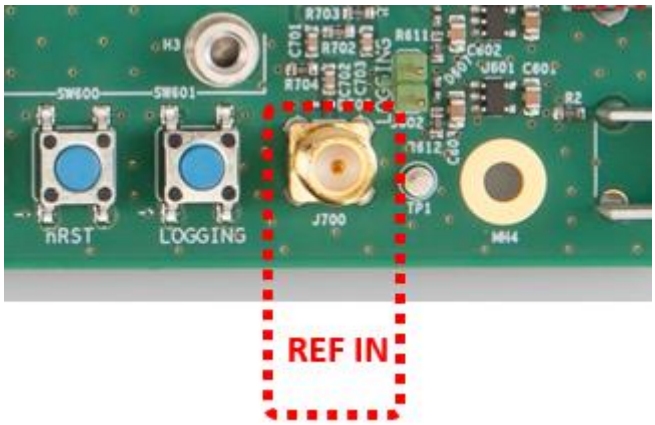
That connector can be attached to a PC to power the DevKit and to communicate with the module over its USB port.

7.9 USB Host

Reserved.

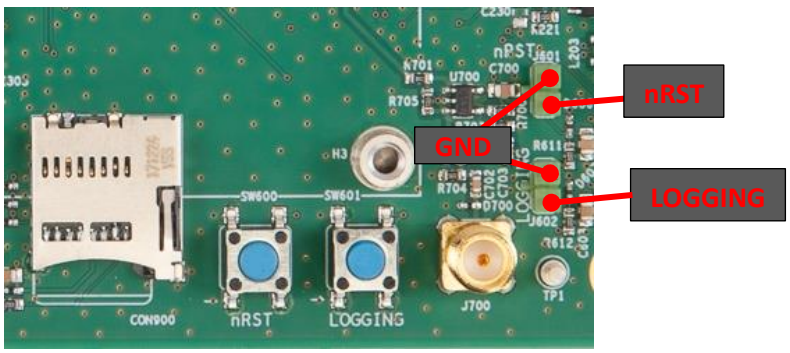
7.10 REF IN

The REF IN SMA connector can be used to feed the module with an external 10-MHz sinusoidal frequency reference.



Input impedance: 50 Ω.
Input level: between -10dBm and +14dBm (0.2Vp-p to 3.2Vp-p).

7.11 Buttons



Pressing the nRST button drives the nRST pin of the mosaic low, which resets the module.

Pressing the LOGGING button drives the LOGBUTTON pin of the mosaic low. This can be used to enabled and disable logging, as described in section 4.6.

The buttons are also connected to J601 and J602 2-pin headers (see above picture). Connecting the nRST or LOGGING pins of these headers to ground is the same as pressing the respective button.

7.12 SD Card Socket

The module can log files on the micro SD Card in this socket. See section 4.6 for a description of the SD Card logging on the mosaic module.

8 Evaluation Kit: mosaic-go

The mosaic-go Evaluation Kit is composed of the mosaic module soldered on an interface board inside a metallic housing.

Mosaic-go part number:

Single-antenna version, incorporating mosaic-X5: **410386** (including accessories).
Dual-antenna version, incorporating mosaic-H: **410397** (including accessories).

Dimensions: 71 x 59 x 12 mm ± 1 mm
Weight: 58 g ± 1 g

8.1 Interfaces

8.1.1 USB

This micro-B connector is used to access the mosaic-go over USB.

It can also be used to power the mosaic-go. See also section 8.4.

8.1.2 RSV USB

This connector is reserved and should not be used.

8.1.3 RF_IN1 and RF_IN2

These are the main and auxiliary antenna connectors, connected to the ANT_1 and ANT_2 pins of the internal mosaic. See section 4.2 for details.

Mosaic-go provides a 5V DC supply to both antenna connectors. In the dual-antenna version, a circuit similar to the one in section 4.2.3.2 is used. The combined main and auxiliary antenna power consumption must not exceed 150mA.

Note that RF_IN2 is only available on the dual-antenna mosaic-go.

8.1.4 TF Card

Socket for a micro SD Card. See section 4.6 for details.

8.1.5 6-pin Connector

Type: GH connector, 1.25mm pitch, 6 way. Mating connector housing: GHR-06V-S

Pin Name	Direction	Level	Description	Comment
VCC	PWR	4.75V-5.5V	Main power supply	
GND		0	Ground	
TXD1	Out	3V3_LVTTL	Serial COM1 transmit line	Directly connects to TXD1 of internal mosaic, see 4.3
RXD1	In	3V3_LVTTL	Serial COM1 receive line	Directly connects to RXD1 of internal mosaic, see 4.3
PPS	Out	3V3_LVTTL	PPS output	PPSO from mosaic converted to 3.3V, see 4.10
EVENT	In	3V3_LVTTL	Event timer input	Connects to EVENTA of mosaic through a 3V3 to 1V8 level translator. See 4.8

8.1.6 4-pin Connector

Type: GH connector, 1.25mm pitch, 4 way. Mating connector housing: GHR-04V-S

Pin Name	Direction	Level	Description	Comment
NRST	In	3V3_LVTTL	Reset input	Directly connects to nRST_IN of internal mosaic, see 4.1
TXD2	Out	3V3_LVTTL	Serial COM2 transmit line	Directly connects to TXD2 of internal mosaic, see 4.3
RXD2	In	3V3_LVTTL	Serial COM2 receive line	Directly connects to RXD2 of internal mosaic, see 4.3
GND		0	Ground	

8.2 Accessories

The following accessories are delivered with mosaic-go:

Accessory	Comment
6-pin COM1 open-ended cable	GH connector in one side and open ended in other side. See wire color code below.
4-pin COM2 open-ended cable	GH connector in one side and open ended in other side. See wire color code below.
USB cable	Micro-B USB cable
Help user guide card	A small printed card which includes the basic how-to guide and QR code to access Septentrio support information.

8.2.1 6-pin COM1 Open-Ended Cable

Pin Name	Wire Color
VCC	red
GND	yellow
TX1	blue
RX1	green
PPS	white
EVENT	black

8.2.2 4-pin COM2 Open-Ended Cable

Pin Name	Wire Color
NRST	red
TXD2	green
RXD2	white
GND	black

8.3 LEDs

The multi-color RGB LED is used to monitor the mosaic-go status. See Appendix A for details.

LEDs	Color Component	Short Description
GPLED	Blue	General purpose LED.
LOGLED	Green	Internal logging status indicator.
POWER	Red	On when mosaic-go is powered.

8.4 Powering the mosaic-go

There are two ways to power the mosaic-go. The nominal input power supply is 5V.

- From the USB connector. This allows powering the board from a PC or from a standard phone-charger adapter. The supported USB voltage range is 4.5V-5.5V.
- Using the VCC pin of the 6-pin connector. The supported voltage range is 4.75V-5.5V.

It is safe to connect both supplies at the same time. Mosaic-go will use the source with the highest voltage.

Note that the power consumption is about 50% higher than the power consumption of the mosaic module alone (see section 3.5).

Appendix A LED Status Indicators

The LED pins can be used to monitor the module status. They can be used to drive external LEDs. It is assumed that the LED lights when the electrical level of the corresponding pin is high.

The general-purpose LEDs (GPLED and GPLED2 pins) are configured with the **setLEDMode** command. The default configuration is:

- GPLED: configured as PVTLED by default;
- GPLED2: configured as RTKLED by default.

The following LED modes are supported.

<table>
<tr><th>GPLED mode</th><th>LED Behaviour</th></tr>
<tr><td>PVTLED</td><td>LED lights when a PVT solution is available.</td></tr>
<tr><td>RTKLED</td><td>LED is off if the PVT is not in RTK mode, blinks in float RTK and is solid on in fixed RTK.</td></tr>
<tr><td>DIFFCORLED</td><td>Differential correction indicator. In rover PVT mode, this LED reports the number of satellites for which differential corrections have been provided in the last received differential correction message (RTCM or CMR).
<table>
<tr><th>LED behaviour</th><th>Number of satellites with corrections</th></tr>
<tr><td>LED is off</td><td>No differential correction message received</td></tr>
<tr><td>blinks fast and continuously (10 times per second)</td><td>0</td></tr>
<tr><td>blinks once, then pauses</td><td>1, 2</td></tr>
<tr><td>blinks twice, then pauses</td><td>3, 4</td></tr>
<tr><td>blinks 3 times, then pauses</td><td>5, 6</td></tr>
<tr><td>blinks 4 times, then pauses</td><td>7, 8</td></tr>
<tr><td>blinks 5 times, then pauses</td><td>9 or more</td></tr>
</table>
The LED is solid ’ON’ when the module is outputting differential corrections as a static base station.</td></tr>
<tr><td>TRACKLED</td><td>
<table>
<tr><th>LED behaviour</th><th>Number of satellites in tracking</th></tr>
<tr><td>blinks fast and continuously (10 times per second)</td><td>0</td></tr>
<tr><td>blinks once, then pauses</td><td>1, 2</td></tr>
<tr><td>blinks twice, then pauses</td><td>3, 4</td></tr>
<tr><td>blinks 3 times, then pauses</td><td>5, 6</td></tr>
<tr><td>blinks 4 times, then pauses</td><td>7, 8</td></tr>
<tr><td>blinks 5 times, then pauses</td><td>9 or more</td></tr>
</table>
</td></tr>
</table>

The LOGLED reports the SD card mount status and logging activity.

LED	LED Behaviour
LOGLED	LED is off when the SD card is not present or not mounted. LED is on when the SD card is present and mounted. Short blinks indicate logging activity.

Appendix B System Noise Figure and C/N0

The system noise figure, in dB, can be calculated as:

$NFsys = 10*\log_{10}(10^{NFant/10} + (10^{NFrx/10}-1)/10^{Gpreamp/10})$

where

- NFant is the antenna LNA noise figure, in dB;
- NFrx is the module noise figure, in dB, as in section 4.2;
- Gpreamp is the net pre-amplification in front of the module, in dB.

For example, with a 2.5-dB antenna LNA noise figure, 30-dB antenna LNA gain and 15-dB cable loss, Gpreamp = 30dB-15dB = 15dB and NRrx is 8.5dB (see table in section 4.2). In this case, the system noise figure is:

$NFsys = 10.\log_{10}(10^{2.5/10}+ (10^{8.5/10}-1)/10^{15/10}) = 2.95$ dB.

The C/N0, in dB-Hz, of a GNSS signal received at a power P can be computed by:

$C/N0 = P - 10.\log_{10}(Tant + 290*(10^{NFsys/10}-1)) + 228.6$ dB

where

- P is the received GNSS signal power including the gain of the antenna passive radiating element, in dBW (e.g. -155dBW)
- Tant is the antenna noise temperature, in Kelvin. Typically Tant = 130K for an open-sky antenna.
- 228.6 is $-10*\log10(k_B)$ with k_B =1.38e-23 J/K the Boltzmann constant.

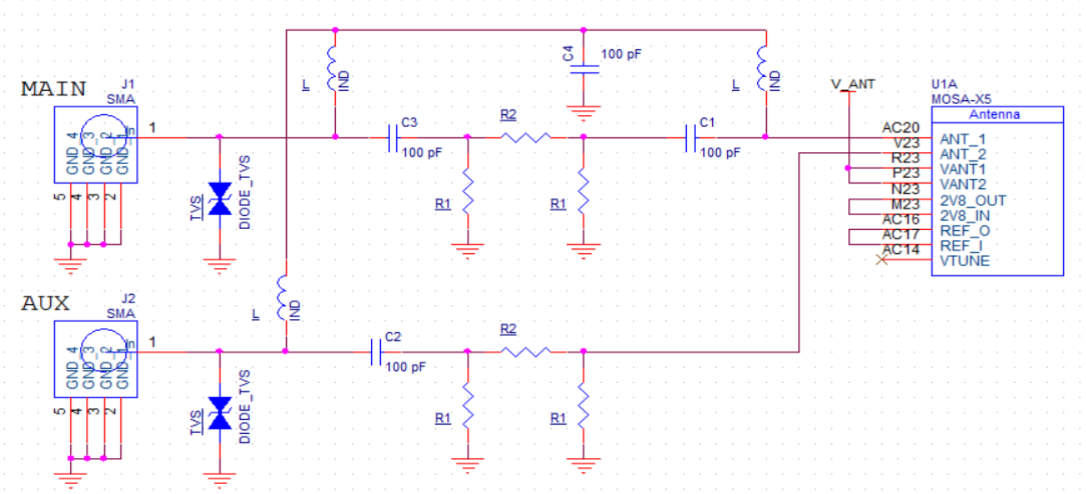
Note that, when connecting the ANT_1 RF input directly to a GNSS simulator, the applicable value for NFsys is 8.5 dB and Tant=290K.

Appendix C mosaic-H RF Gain Adjustment

This appendix in only applicable to the dual-antenna mosaic-H module.

The pre-amplification in front of the mosaic-H is required to be between 15 and 35 dB (AGC gain reported by the receiver between 30 and 50dB). This is net pre-amplification, equal to the active gain of the antenna minus losses in the coax cables at 1.6 GHz. Above 35 dB of pre-amplification, the cross-talk of the auxiliary antenna into the main antenna could degrade performance.

Applications which work with high gain antennas shall use in-line attenuators. These can be implemented on the PCB as indicated in the figure below.



- TVS diode: use SESD0402X1BN-0010-098 or equivalent
- Inductor L: select an inductor which is self-resonant between 1350 and 1450 MHz, with at least 300 mA current rating, e.g. Würth 744786139A
- Avoid stubs at the RF path. The inductors, TVS diodes and R1 resistors shall be very close to the RF trace, and have short grounding if applicable.

If the target attenuation is A dB, the resistors R1 and R2 can be dimensioned as follows, rounding to the nearest E12[3] value:

$$R1 = 50.\frac{1 + 10^{-A/20}}{1 - 10^{-A/20}}\ Ohm$$

$$R2 = \frac{5000.R1}{R1^2 - 2500}\ Ohm$$

The table below shows R1 and R2 values for some common attenuations:

Attenuation [dB]	R1 [Ohm]	R2 [Ohm]
6	150	39
10	100	68
20	56	220

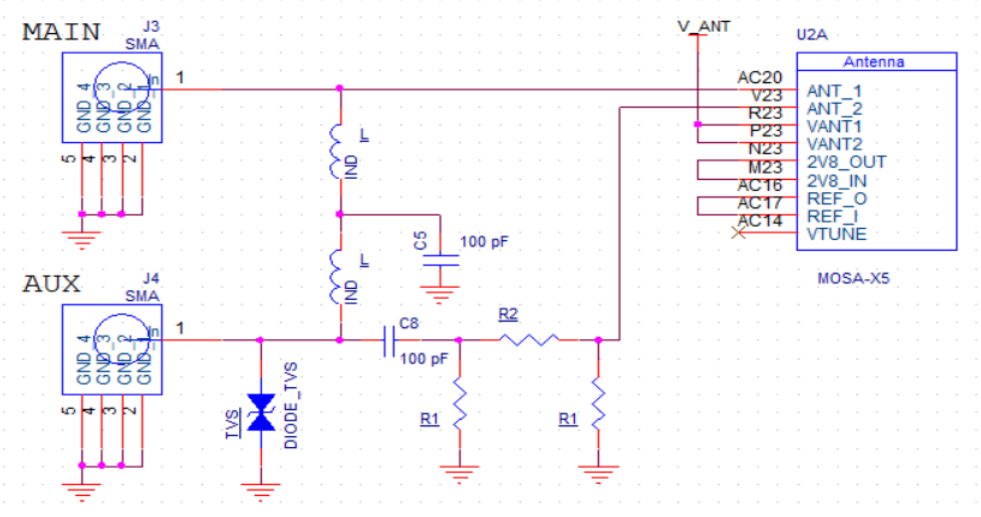
[3] E12 series multipliers of a power of ten: 1.0, 1.2, 1.5, ,1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2

In case a 10-dB attenuator is inserted, the supported net pre-amplification range would be 25-45 dB. If the design is intended for one particular target configuration, for instance with 45 dB pre-amplification, it is recommended to optimize the attenuator towards a 25 dB net pre-amplification in front of the module. In the example of a 45 dB pre-amplification, a 20 dB attenuation shall be targeted.

The difference in pre-amplification in front of the main and auxiliary inputs of the module shall be less than 5 dB. Higher mismatch could induce cross-talk between the signals of both antennas, which could get significant compared to typical errors induced by reflections and antenna non-idealities. When using identical antennas for the main and auxiliary input, differences between pre-amplification usually relate to differences in cable lengths. For example, RG58 cable will typically have between 0.5 and 0.8 dB/m loss at the GNSS operating frequencies (consider 1.6 GHz). Therefore, RG58 cable length differences beyond 6 m could cause issues.

In applications with limited asymmetry between both pre-amplifications (<5 dB), it is recommended to route the stronger signal to the main antenna input and the weaker signal to the auxiliary antenna input of the module. The circuit in section 4.2.3.2 is then sufficient.

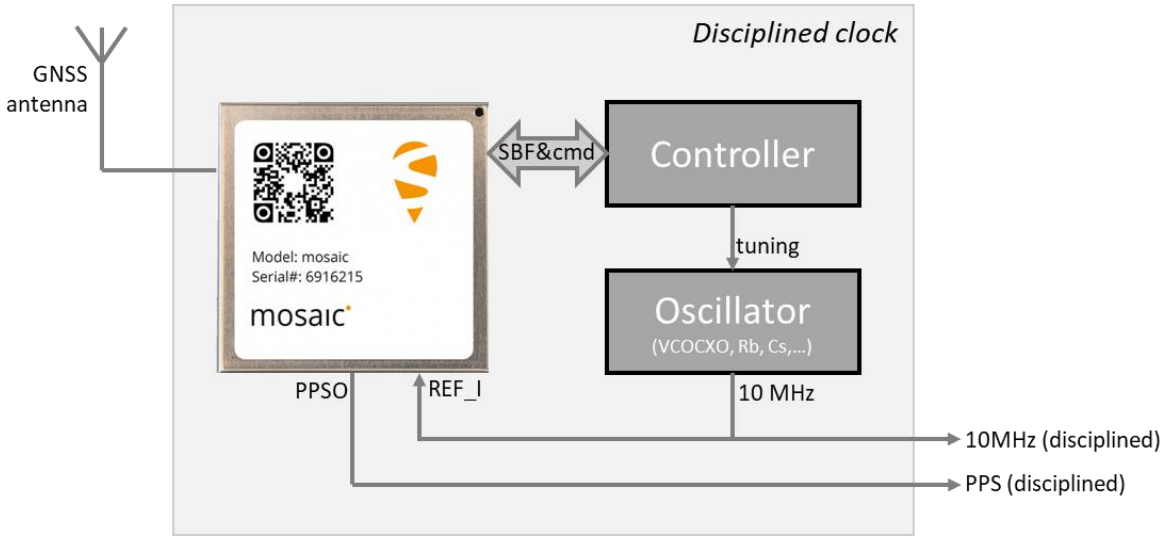
In applications with a more substantial asymmetry, an attenuator circuit is to be inserted to reduce the strongest signal to the level of the weaker one. An example is shown in the figure below, in which case the strongest signal would be at the AUX connector. R1 and R2 shall be dimensioned as explained earlier, targeting an attenuation equal to the expected difference between the pre-amplifications.



Appendix D mosaic-Based Disciplined Clock

This appendix is only applicable to modules where the Frequency Sync permission is enabled. It describes a possible architecture of a 10-MHz disciplined clock using the mosaic as precise time source. This architecture is particularly suitable in combination with Fugro AtomiChron™ precise time service.

The proposed disciplined clock architecture is shown below. The mosaic uses the 10-MHz signal from the steered oscillator as frequency reference, instead of its own internal crystal oscillator (the internal oscillator is turned off). A controller reads the clock bias reported by the module in its SBF messages and steers it to zero by adjusting the frequency of the oscillator. When the clock bias is zero, the receiver time scale is aligned with GNSS time. The PPSO pulses from the module are configured to follow the receiver time scale. Unlike traditional approaches, this architecture does not require any hardware to measure time delays. It is also not affected by any PPS resolution limitation (a.k.a "saw tooth" effect).



Before use, configure the mosaic so that it starts-up with the PPS pulses disabled, and that it performs an initial precise synchronization to GNSS time. This is done by entering the following user commands:

- **setPPSParameters, off**
- **setClockSyncThreshold, usec500, on**
- **exeCopyConfigFile, Current, Boot**

See the Reference Guide for a detailed description of these commands. The commands above have to be entered only once, as the last "**exeCopyConfigFile**" command makes them persistent in the boot configuration.

At each subsequent (re)start of the system, the controller runs the following algorithm:

1. First, enable the output of the `PVTCartesian` (or `PVTGeodetic`) and of the `ReceiverTime` SBF block to the controller at the desired rate, say, 1Hz.
2. Wait until the `FINETIME` bit is set in the `SyncLevel` field of `ReceiverTime`, indicating that the receiver time initialization is complete.

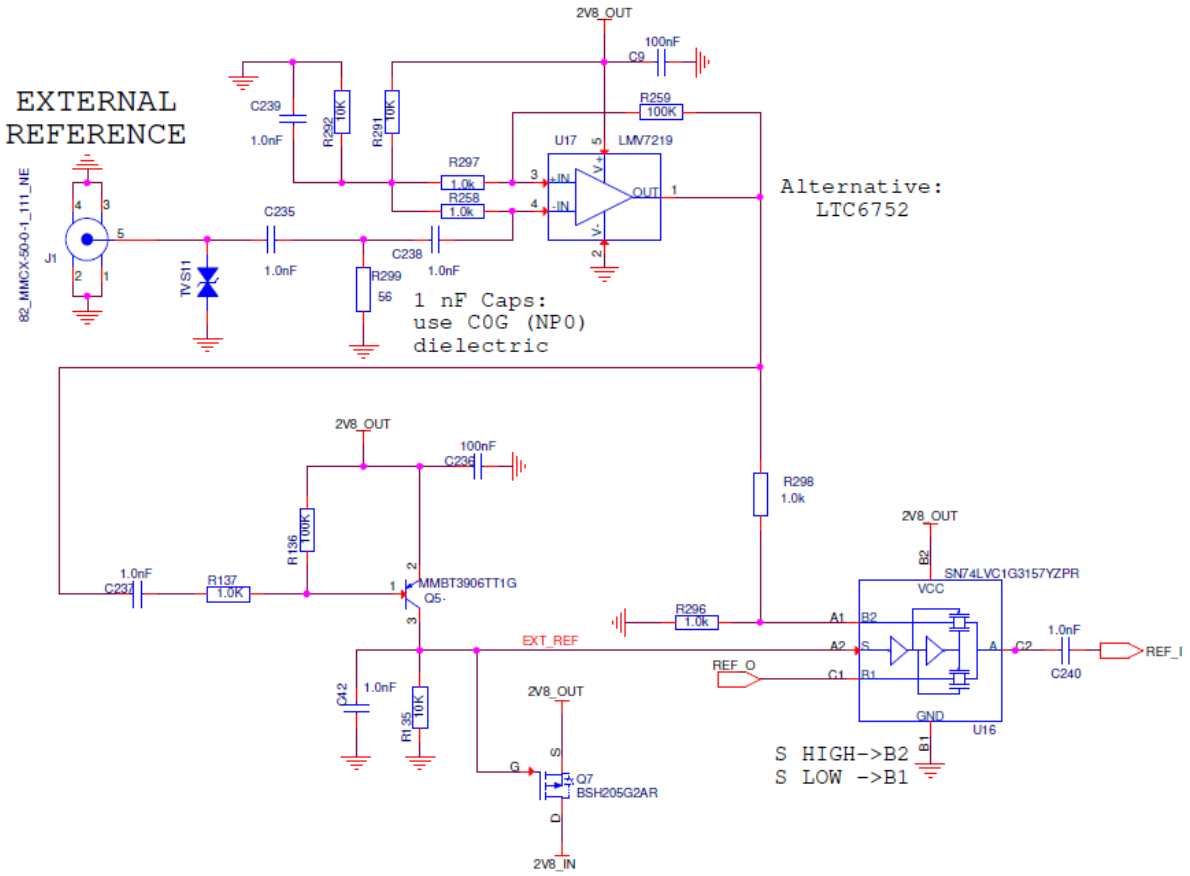
3. Each time the `PVTCartesian` block is received by the controller, read the clock bias from its `RxClkBias` field.
4. The initial clock bias is small (typically < 200ns) thanks to the initial precise synchronization. If it is positive, adjust the tuning level to slightly decrease the oscillator frequency. If it is negative, slightly increase the oscillator frequency. Continue this process until the clock bias has converged to zero. While steering the oscillator frequency, it is recommended to keep the rate of frequency change smaller than 3 ppb per second, i.e. not to change the 10-MHz frequency by more than 0.03 Hz per second.
5. When lock is achieved, the receiver time is synchronized with GNSS time. It is time to enable the PPS from the mosaic in "RxClock" mode (using the **setPPSParameters** command). In RxClock mode, the PPS pulses are aligned with the receiver time, itself locked to the 10-MHz reference from the oscillator. More specifically, the pulses are generated exactly every 10 million cycles of the oscillator (assuming a 1-Hz PPS rate), so they keep a constant phase with respect to the oscillator cycles.
6. Continue steering the clock bias to zero to keep the oscillator and the PPS aligned with GNSS time.
7. During GNSS outages, the PPS pulses from the module remain phase locked to the oscillator, ensuring seamless hold-over.

The PPS aligned as described above will typically be late by a few tens of nanoseconds. This is due to delays in the antenna, cables and RF frontend of the receiver. In the mosaic modules, the frontend RF delay is about 10 ns. Typical values for the antenna delay range from 10 to 20 ns, and coax cable delay amounts to about 5 ns per meter. If the total delay *D* is known, it can be compensated with the **setCalibCommonDelay** user command.

When using Fugro's AtomiChron™, the clock bias refers to a GNSS (typically GPS) time scale during the first two to three minutes after start up, before switching to the AtomiChron™ time scale. The change of reference time scale from GPS to AtomiChron™ may lead to a clock bias shift by a couple of nanoseconds. The reference time scale is reported in the `TimeSystem` field of the `PVTCartesian` SBF block and the jump can be avoided by waiting until that field is set to "Fugro AtomiChron".

Appendix E Frequency Reference Detection

Section 4.7.2 describes how to use the mosaic with an external frequency reference. In cases where the external frequency reference is optional, a detection circuit may be useful. An example of such circuit is described here.



With the above circuit, the module uses the external 10-MHz reference provided at the EXTERNAL REFERENCE connector if a suitable signal is detected. In the absence of external reference, it enables its internal reference. More specifically:

- if there is a valid signal at the EXTERNAL REFERENCE connector (input impedance 50Ω, detection level -14dBm, max supported level +12dBm), EXT_REF is high, 2V8_IN is floating and the external reference is routed to REF_I through U17 and U16;
- otherwise, EXT_REF is low, 2V8_IN is connected to 2V8_OUT through Q7 and REF_I is fed with REF_O through U16.

The connections to the module are the 2V8_IN, 2V8_OUT, REF_I and REF_O pins described in section 4.7. Note that the signal path includes 1nF capacitors. It is important to use C0G (NP0) types to avoid piezoelectric effects.

⚠ Switching between external and internal frequency reference must occur when the module is powered off, or the module must be reset after switching.

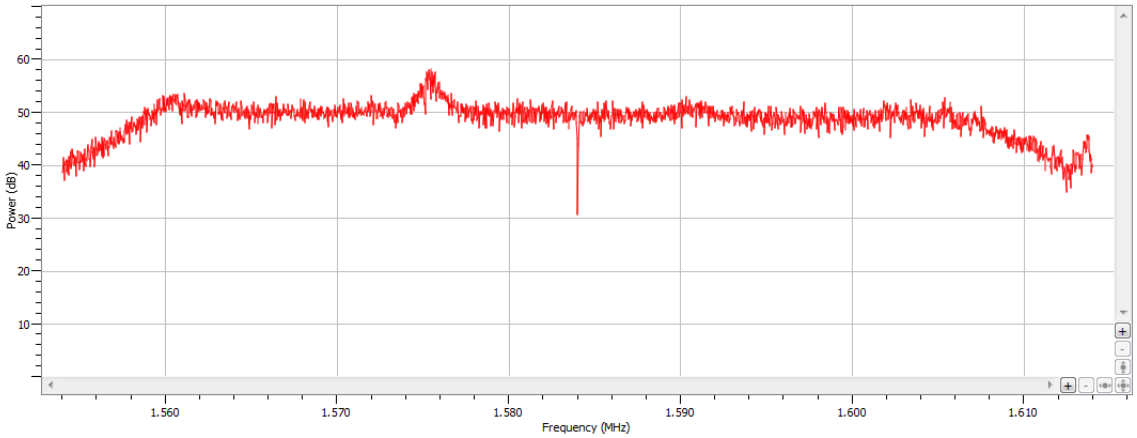
Appendix F EMC Considerations

In applications in which the electronics are collocated with the GNSS antenna, cross-talk could be a major concern. GNSS signals are very weak and easily interfered by radiated harmonics of digital signals.

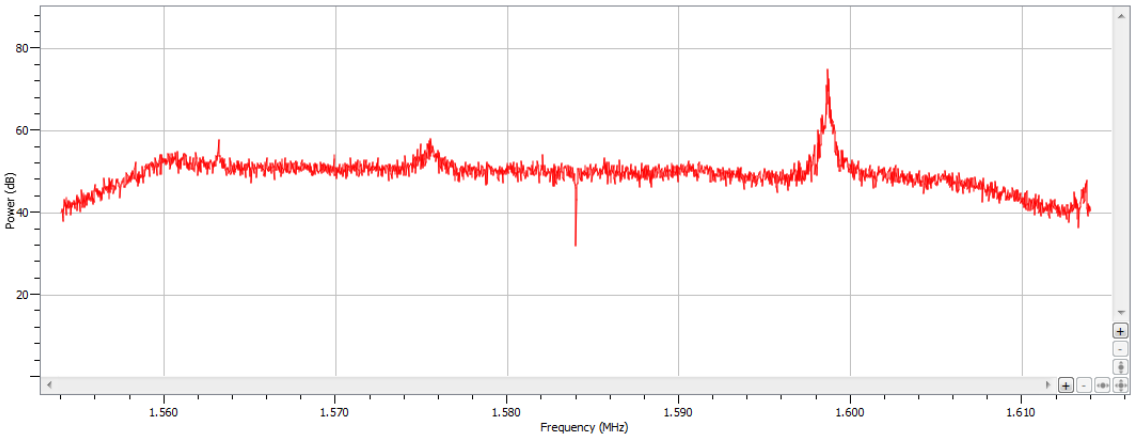
The most useful indicator of the signal reception quality is the C/N0 of the satellites in view. The C/N0 can be viewed in the RxControl graphical interface by clicking *View / Carrier to Noise Plot*. In open-sky conditions, the C/N0 values should reach up to 50 dB-Hz for the strong signals on L1 and L5, and up to 45 dB-Hz on L2, as illustrated below.

If the maximum C/N0 is lower than expected, interference and cross-talk from nearby electronics is likely, and the source of the problem needs to be identified. This is where the RF spectrum monitor built in the GNSS receiver comes in handy. The spectrum monitor can be accessed in RxControl under the *View / Spectrum View* menu. The spectrum can also be monitored offline if the `BBSamples` SBF blocks are logged.

The figure below shows a clean open-sky L1-band spectrum. The bump at 1575MHz corresponds to the GNSS signals at the L1/E1 frequency, and is normal.

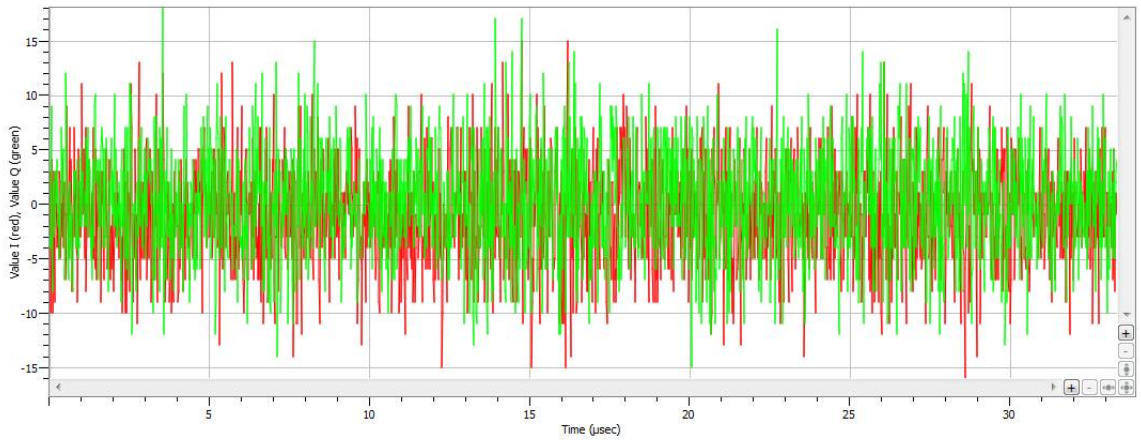


An example of interference is shown below. This particular interference at about 1598 MHz falls in the GLONASS L1 band and slightly degrades the L1 C/N0 of some GLONASS satellites.

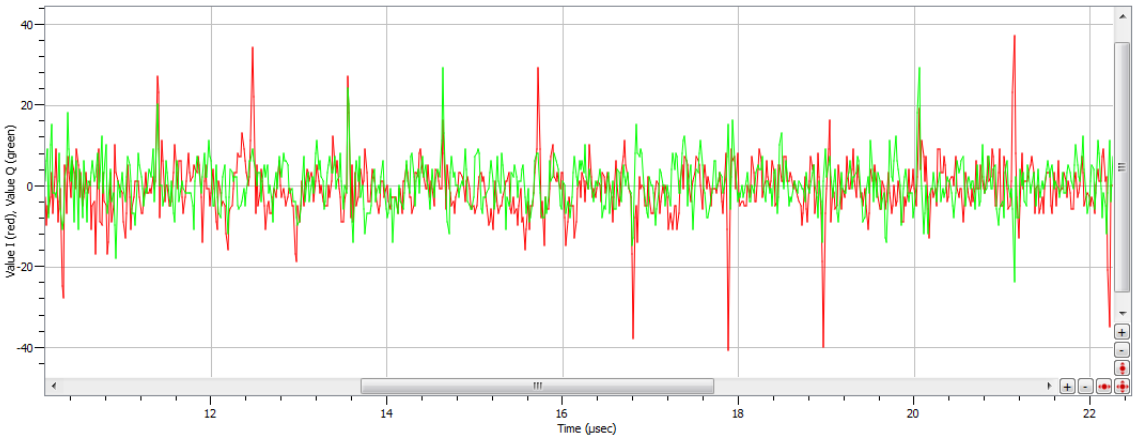


Try to keep personal computers and other equipment more than 2 meters away from the antenna while assessing electromagnetic compatibility of the integration.

RxControl also allows to observe the time domain signal. This should look like white Gaussian noise as illustrated below.



Intermittent interference (µs-scale) has little impact if its duty cycle is below 10%. For example, these short pulses from a digital circuit close to the antenna are essentially harmless.



If interference is detected, look for the root cause by switching off devices. Typical sources of interference are:

- Unshielded flat cables carrying digital signals or power signals towards digital circuits. Particularly, cable joints tend to radiate.
- High-speed digital devices, such as application processors, modems and cameras.
- Digital signals on the application board (e.g. clock signals, SDIO signals).

If spectral peaks are observed in the spectrum, this usually relates to radiated harmonics. The source can be identified by looking for an integer relation between the observed spectral peaks and the system frequencies. For example, peaks at 1200 and 1248 MHz are an indication of an interfering source at 48 MHz as this maps to the 25th and 26th harmonic of a 48 MHz signal. This may correspond to the frequency of a microcontroller in the application.

Integration cross-talk can be solved in a number of ways:

- Shift the clock frequency of the interfering signal to avoid the GNSS bands.
- Use shielding tape with conductive adhesive.
- Shield radiating circuits, preferably all around.
- Put digital signals in inner layers of the application board.
- Change the antenna location by experimentation.
- Enable the interference mitigation feature of the GNSS receiver. Narrow spectral peaks can be eliminated with the notch filters (see the **setNotchFiltering** command). Intermittent wide-band cross-talk can often be eliminated with the wide band interference canceller (see the **setWBIMitigation** command).

The mosaic module has been designed to minimize radiation and can be used close to an antenna without additional shielding.

It is up to the integrator to ensure EMC regulations of the end-product are met. For this please respect the guidelines of section 5.5.4.

Appendix G Pad List

A2	RTC_XTALO
A3	RTC_XTALI
A4	GND
A5	USB_DEV_P
A6	USB_DEV_N
A7	GND
A8	USB_VBUS1
A9	Reserved_NC
A10	ONOFF
A11	nRST_IN
A12	MODULE_RDY
A13	Reserved_NC
A14	GPLED
A15	GND
A16	GND
A17	GND
A18	VDD_3V3
A19	VDD_3V3
A20	VDD_3V3
A21	GND
A22	GND
A23	GND
B1	RXD1
B2	LOGLED
B3	Reserved_NC
B4	GND
B5	GND
B6	GND
B7	GND
B8	VDD_BAT
B9	Reserved_NC
B10	Reserved_NC
B11	Reserved_NC
B12	Reserved_NC
B13	GND
B14	Reserved_NC
B15	Reserved_NC
B16	PMIC_ON_REQ
B17	GND
B18	VDD_3V3
B19	VDD_3V3
B20	VDD_3V3
B21	GND
B22	Reserved_NC
B23	Reserved_NC
C1	RTS1
C2	Reserved_NC
C3	Reserved_NC
C4	GND
C5	Reserved_NC
C6	Reserved_NC
C7	GND
C8	Reserved_NC
C9	Reserved_NC
C10	Reserved_NC
C11	Reserved_NC
C12	Reserved_NC
C13	Reserved_NC
C14	Reserved_NC
C15	GND
C16	GND
C17	GND
C18	VDD_3V3
C19	VDD_3V3
C20	VDD_3V3
C21	Reserved_NC
C22	Reserved_NC
C23	GND
D1	TXD1
D2	GND
D3	RXD4
D21	GND
D22	GND
D23	GND
E1	CTS1
E2	GND
E3	TXD4
E21	GND
E22	GND
E23	GND
F1	RXD2
F2	nRST_LAN
F3	Reserved_NC
F21	GND
F22	GND
F23	GND
G1	RTS2
G2	GND
G3	Reserved_NC
G21	GND
G22	Reserved_NC
G23	GND
H1	TXD2
H2	RMII_TXD1
H3	Reserved_NC
H21	GND
H22	GND
H23	GND
J1	CTS2
J2	RMII_TXD0
J3	Reserved_NC
J21	GND
J22	GND
J23	GND
K1	RXD3
K2	GND
K3	LOGBUTTON
K21	GND
K22	GND
K23	GND
L1	RTS3
L2	RMII_TXEN
L3	GP2
L21	GND
L22	GND
L23	GND
M1	TXD3
M2	RMII_RXER
M3	GPLED2
M21	GND
M22	GND
M23	2V8_IN
N1	CTS3
N2	RMII_CRSDV
N3	Reserved_NC
N21	GND
N22	GND
N23	2V8_OUT
P1	GND
P2	GND
P3	GND
P21	GND
P22	GND
P23	VANT
R1	Reserved_NC
R2	RMII_RXD0
R3	GND
R21	GND
R22	GND
R23	VANT
T1	Reserved_NC
T2	RMII_RXD1
T3	Reserved_NC
T21	GND
T22	GND
T23	GND
U1	Reserved_NC
U2	GND
U3	Reserved_NC
U21	GND
U22	GND
U23	GND
V1	Reserved_NC
V2	MDC
V3	Reserved_NC
V21	GND
V22	GND
V23	ANT_2
W1	Reserved_NC
W2	MDIO
W3	Reserved_NC
W21	GND
W22	GND
W23	GND
Y1	SD1_DATA0
Y2	GND
Y3	Reserved_NC
Y21	GND
Y22	GND
Y23	GND
AA1	SD1_CLK
AA2	RMII_CLK
AA3	Reserved_NC
AA4	GP1
AA5	Reserved_NC
AA6	Reserved_NC
AA7	Reserved_NC
AA8	Reserved_NC
AA9	Reserved_NC
AA10	Reserved_NC
AA11	Reserved_NC
AA12	Reserved_NC
AA13	GND
AA14	GND
AA15	GND
AA16	GND
AA17	GND
AA18	GND
AA19	GND
AA20	GND
AA21	GND
AA22	GND
AA23	GND
AB1	SD1_CMD
AB2	GND
AB3	GND
AB4	GND
AB5	GND
AB6	GND
AB7	Reserved_GND
AB8	GND
AB9	Reserved_NC
AB10	Reserved_NC
AB11	Reserved_NC
AB12	Reserved_NC
AB13	GND
AB14	GND
AB15	GND
AB16	GND
AB17	GND
AB18	GND
AB19	GND
AB20	GND
AB21	GND
AB22	GND
AB23	GND
AC1	Reserved_NC
AC2	Reserved_NC
AC3	SYNC
AC4	1V8_OUT
AC5	Reserved_NC
AC6	EVENTA
AC7	EVENTB
AC8	PPSO
AC9	Reserved_NC
AC10	Reserved_NC
AC11	Reserved_NC
AC12	Reserved_NC
AC13	GND
AC14	VTUNE
AC15	GND
AC16	REF_O
AC17	REF_I
AC18	GND
AC19	GND
AC20	ANT_1
AC21	GND
AC22	GND
AC23	GND